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05	CPU LGA1151-B-DDR4
06	CPU LGA1151-C
07	CPU LGA1151-D
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09	DDR4 CHANNEL B
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SHEET TITLE

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6

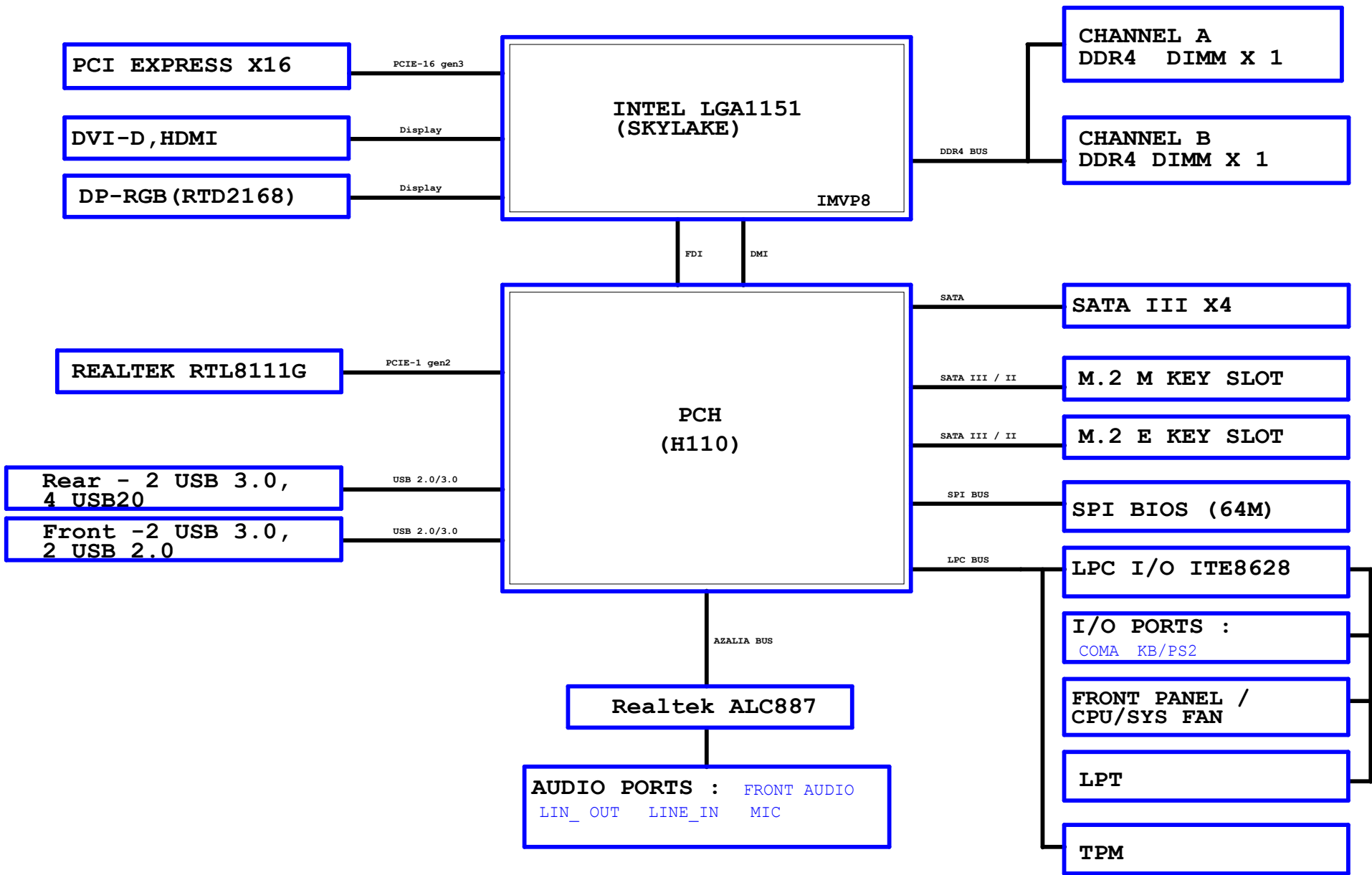
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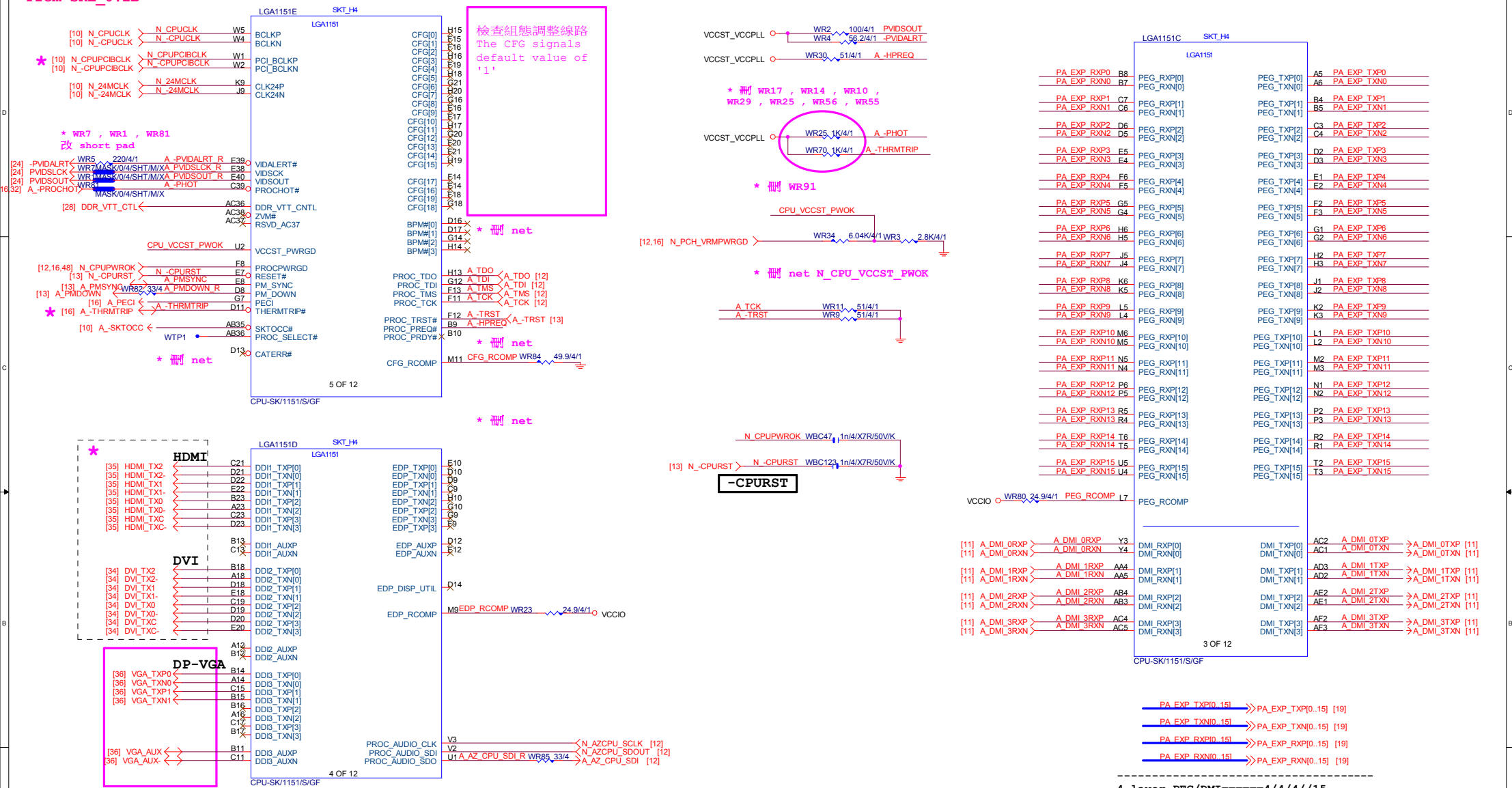
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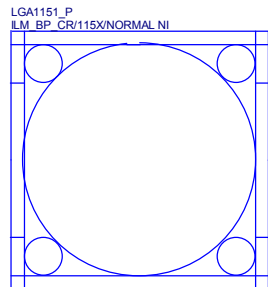
BLOCK DIAGRAM



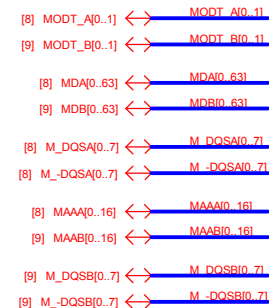
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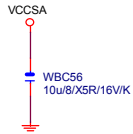


* 改DDR4 net



Need check the new CPU ME

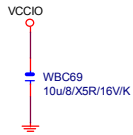




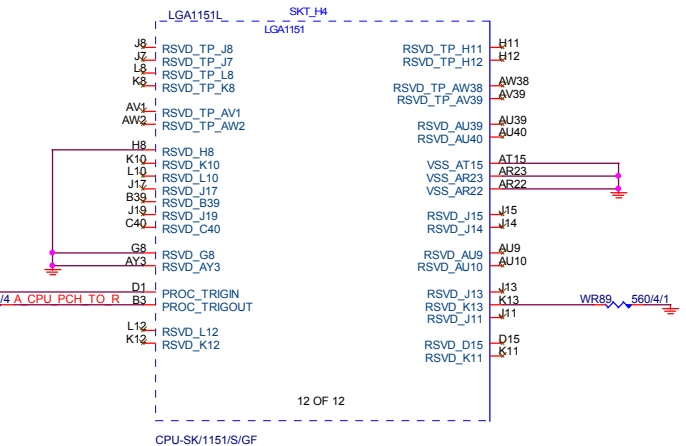
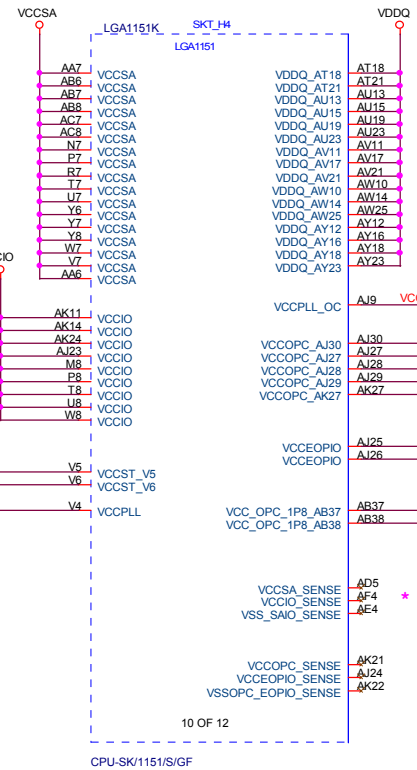
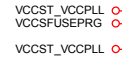
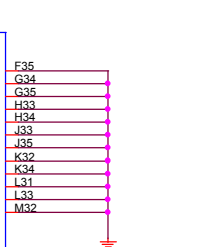
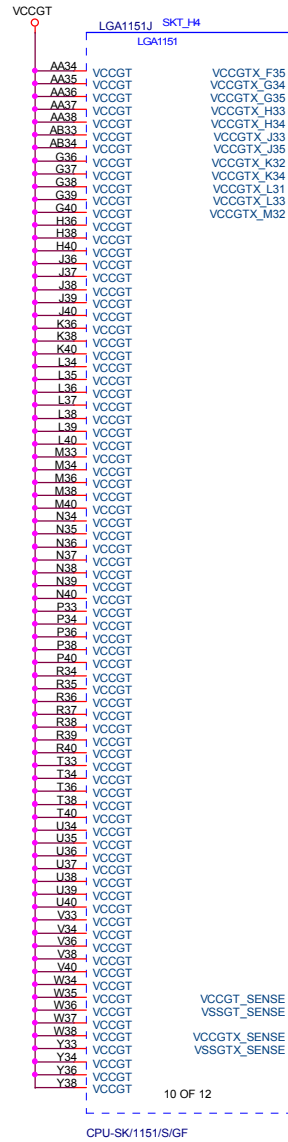
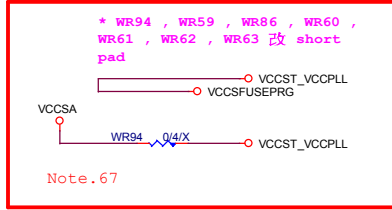
* 刪 WBC50 電容

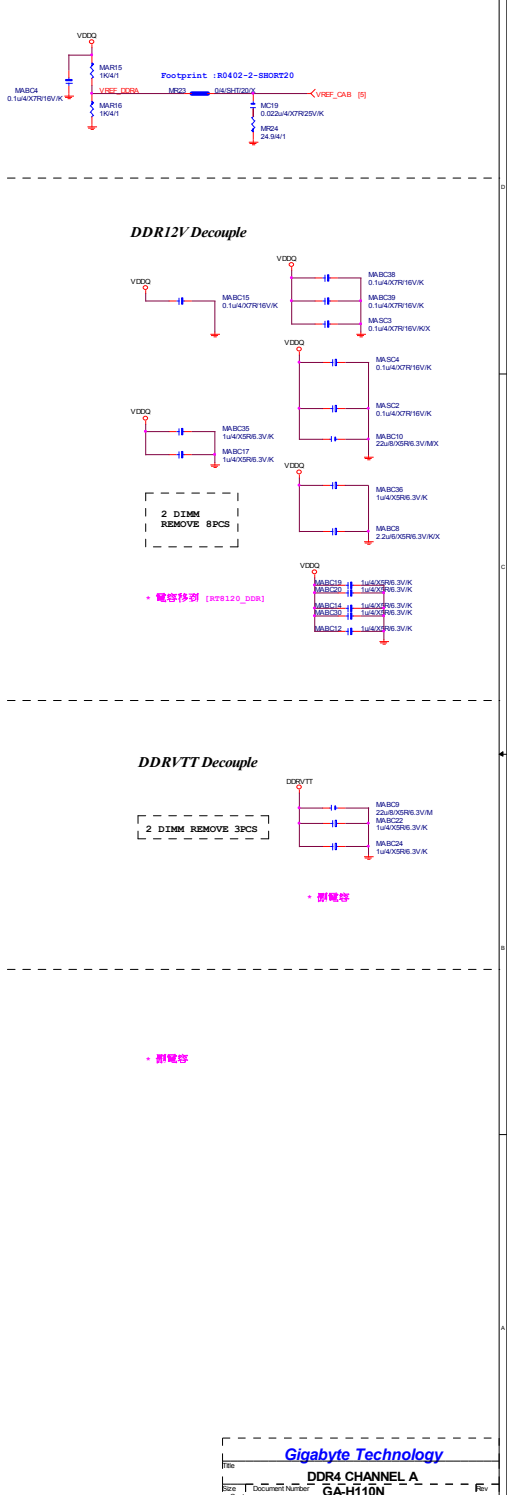
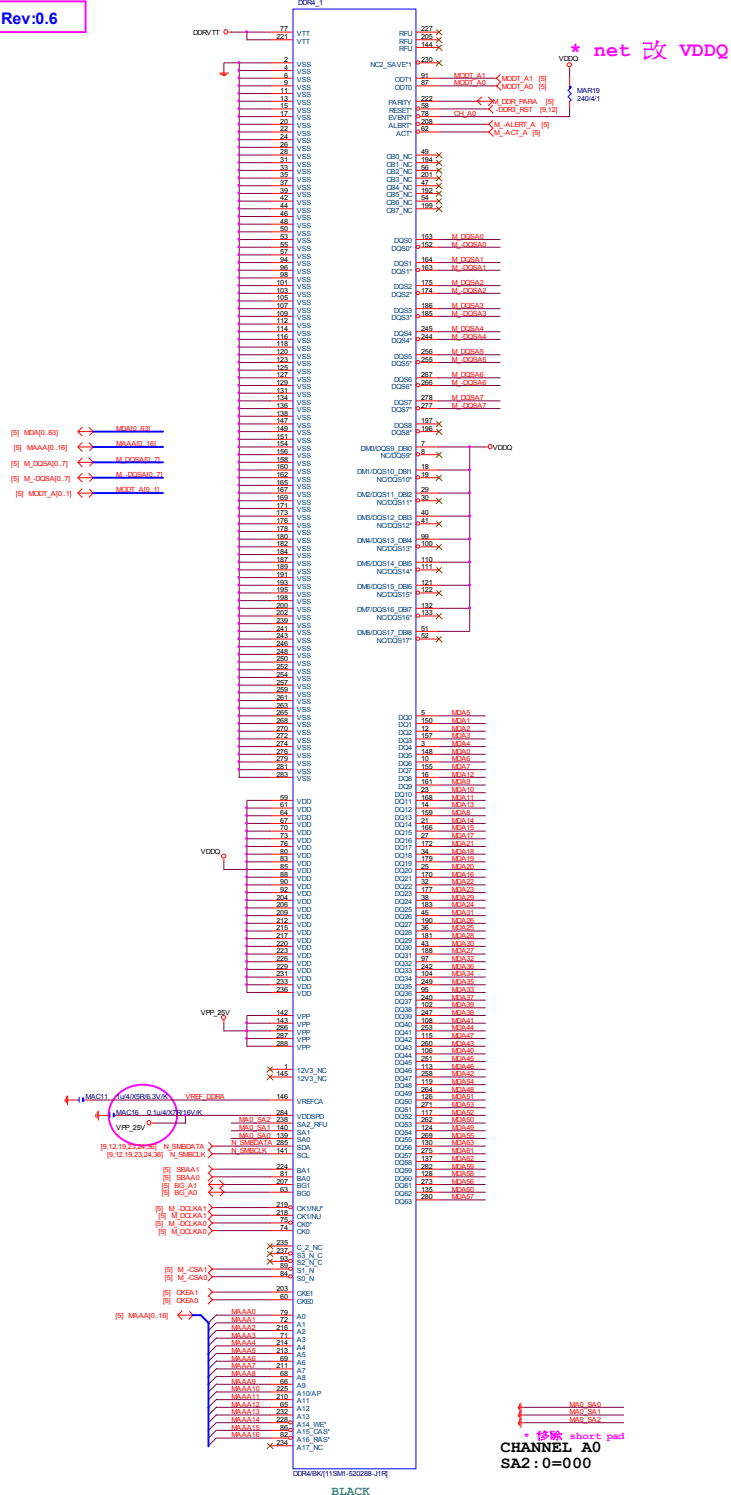
* WBC51 , WBC52
VDDQ 改 VCCSA

* 刪 WBC124 , WBC125 , WBC126 , WBC127 電容

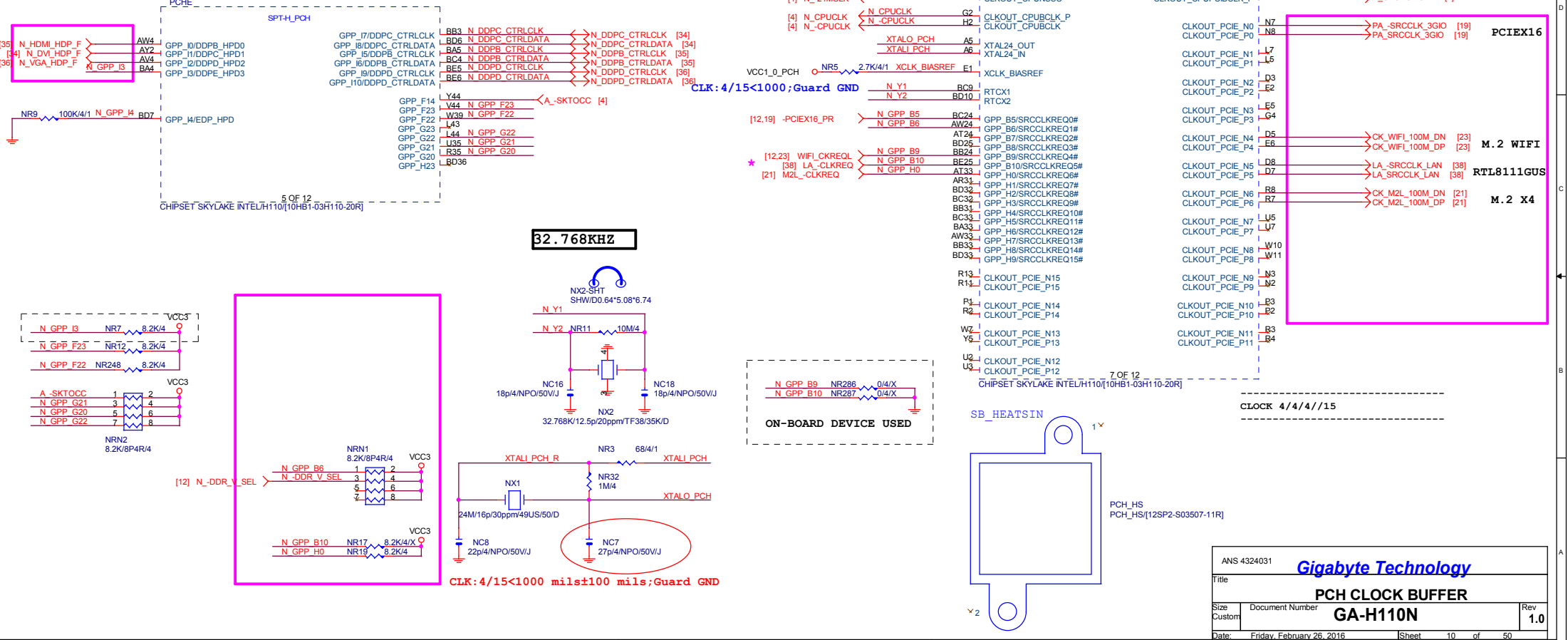


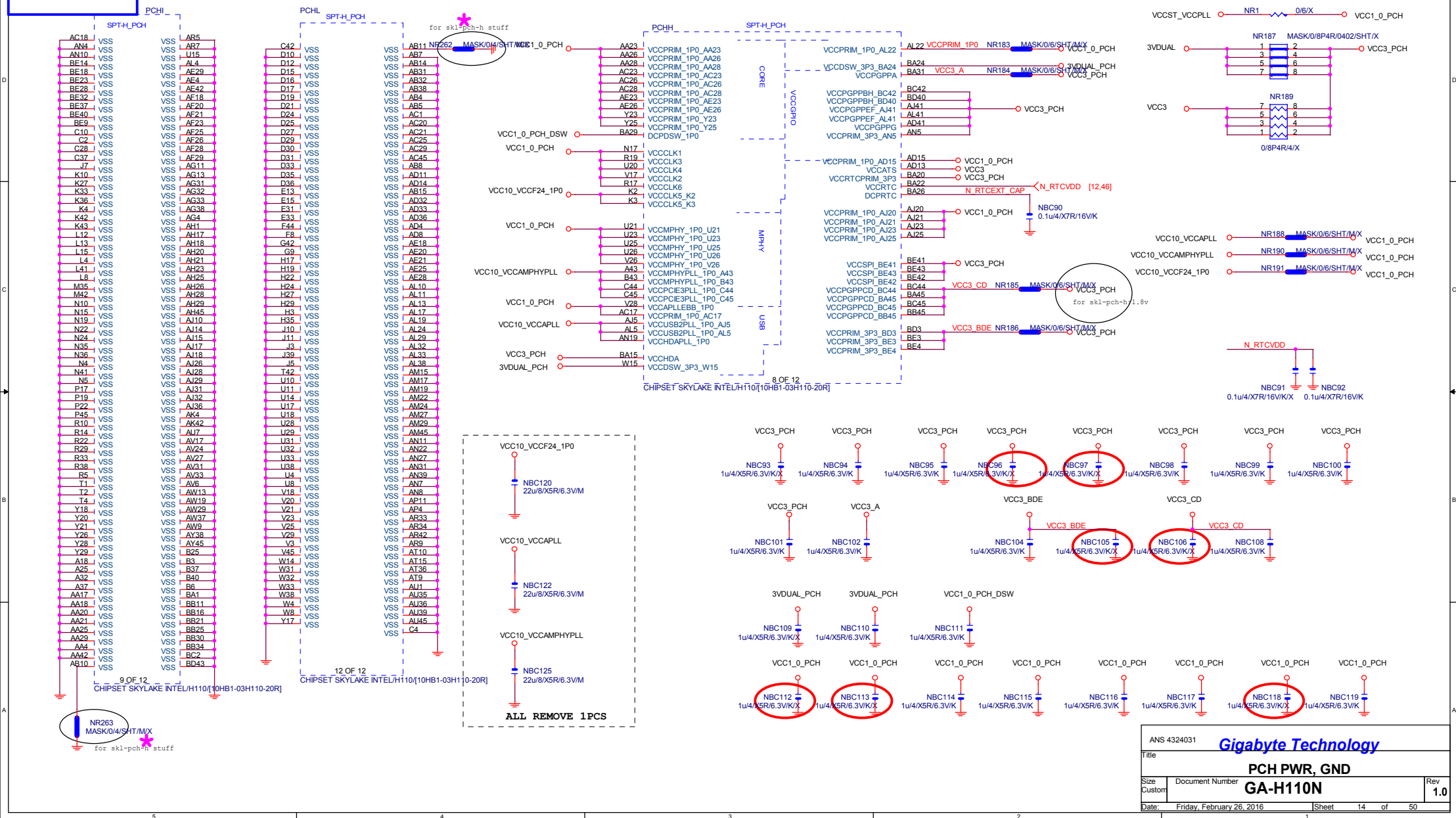
* 刪 VCCGT 電容

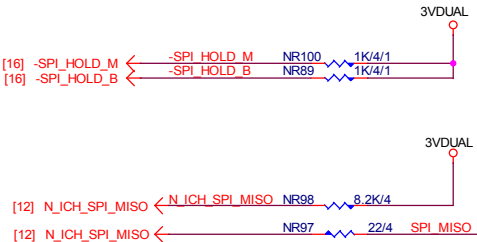
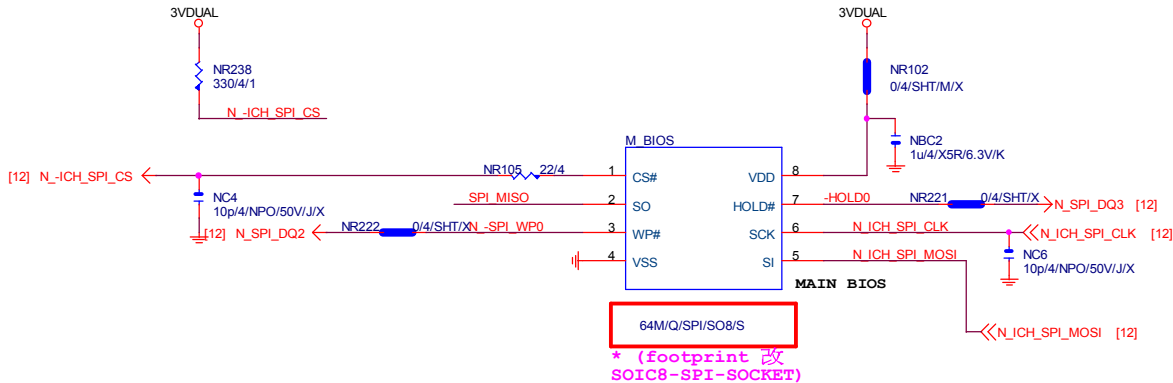




Rev 0.7



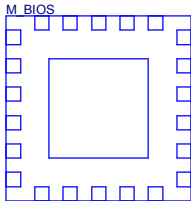




BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

Remove NBC4

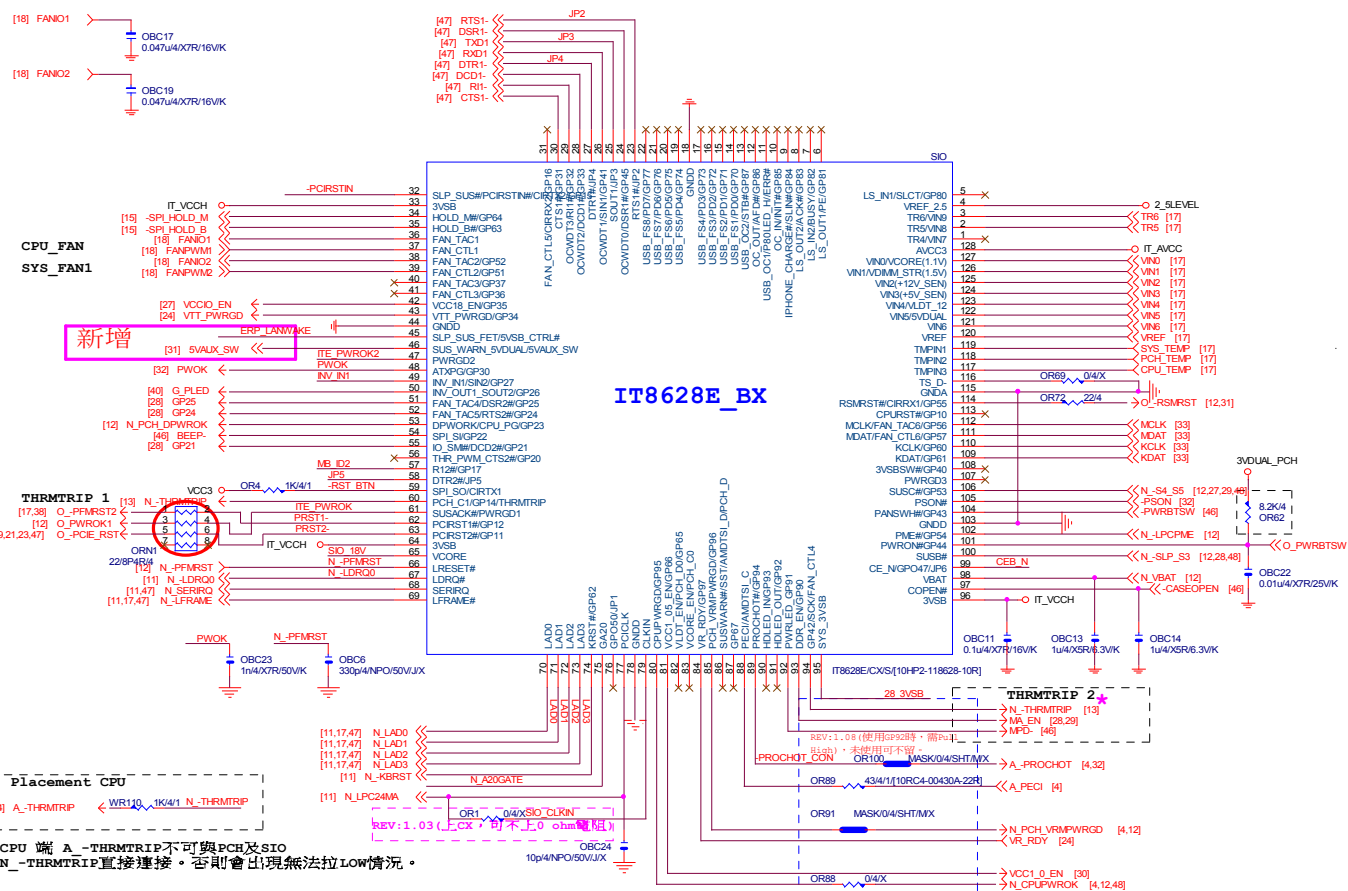
1 means floating
0 means PD 1K



LCP/G-FL/1.27mm/200MIL/WHITE[10SL2-000008-31R]/X

* 試産先上 , PVT 移除

SIO IT8628cX REV:1.08



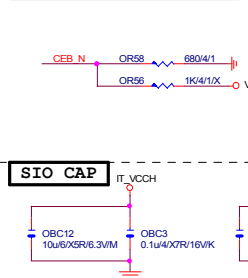
FAN TABLE

CPU_FAN	FAN_CTL1
FAN_TAC1	FAN_TAC1
SYS_FAN1	FAN_CTL2
FAN_TAC2	FAN_TAC2
SYS_FAN2	FAN_CTL3
FAN_TAC3	FAN_TAC3
SYS_FAN3	FAN_CTL4
FAN_TAC4	FAN_TAC4
OPT_FAN or SYS_FAN4	N/A
THRMTRIP1	YES PIN56
THRMTRIP2	YES PIN31

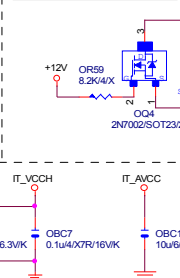
IT8620E GPIO問題匯整

PIN 50	GP26-第一次接上POWER時會拉LO
PIN 90/91	DEFAULT為HIDLED FUNCTION, GP93 BYPASS TO GP92 高電阻時 GP92 會被拉LO (ITE BUG)
PIN 108	GP40--- POWER ON 時會拉LO
PIN 111/112	MOUSE 限FAN6 FUNCTION 標一使用, 不然會互相干擾
PIN 22	PIN22, 轉高於3V, 若低於此部分COM POINT及LPT裝置 轉噪器會異常動作。

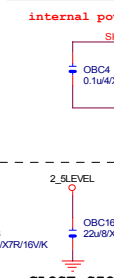
DUAL BIOS OPT STRAP



Power leakage



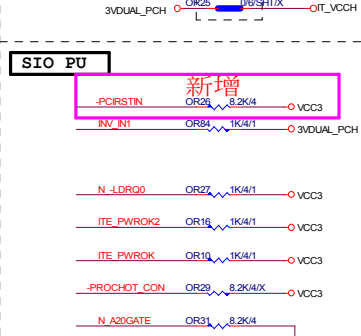
SIO 18V



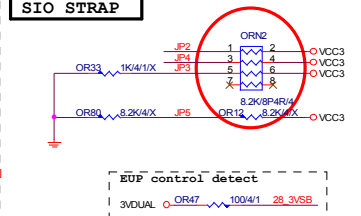
SIO CAP



PWR SHT



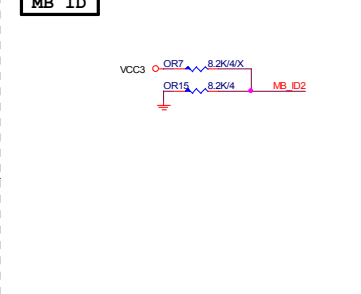
SIO PU



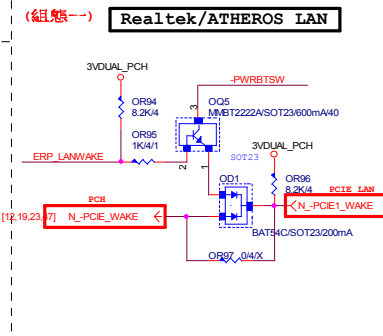
ERP control detect

JP2	1	Disable WDT
JP2	0	Enable WDT to test PWR0K
JP3	1	SPI-Flash Disable
JP3	0	SPI-Flash Enable
JP4	1	k8 power sequency function is Disable
JP4	0	k8 power sequency function is Enable
JP5	1	anti-surge Disable
JP5	0	anti-surge Enable
JP3	1 1	The default value of EC Index 63h/68h/73h is 80h.
JP3	1 0	The default value of EC Index 63h/68h/73h is FFh.
JP5	0 1	The default value of EC Index 63h/68h/73h is 00h.
JP5	0 0	The default value of EC Index 63h/68h/73h is 40h.

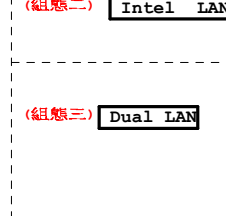
MB ID



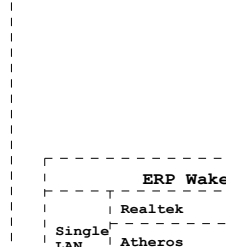
ERP WAKE on LAN (依LAN組態選擇)



Intel LAN



Dual LAN

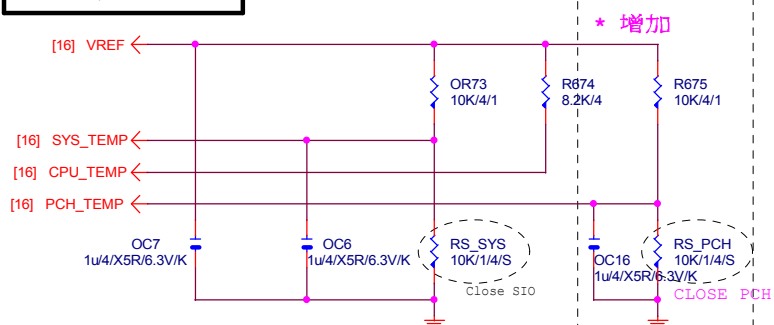


ERP Wake on LAN

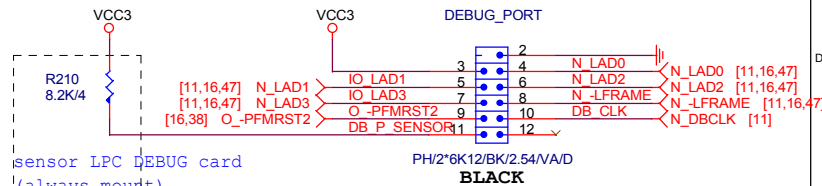
Single LAN	Realtek	組態一
Dual LAN	Atheros	組態二
	Intel 219	
Dual LAN	Atheros+Atheros	組態一
	Intel 219+Intel 210	
No Support ERP	BOM不上	N/A

REV:1.07

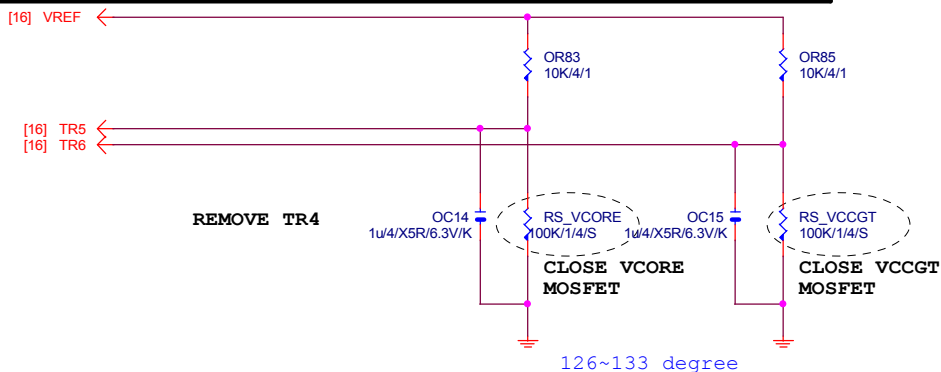
TEMP H/W MONITOR



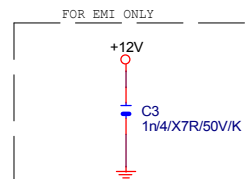
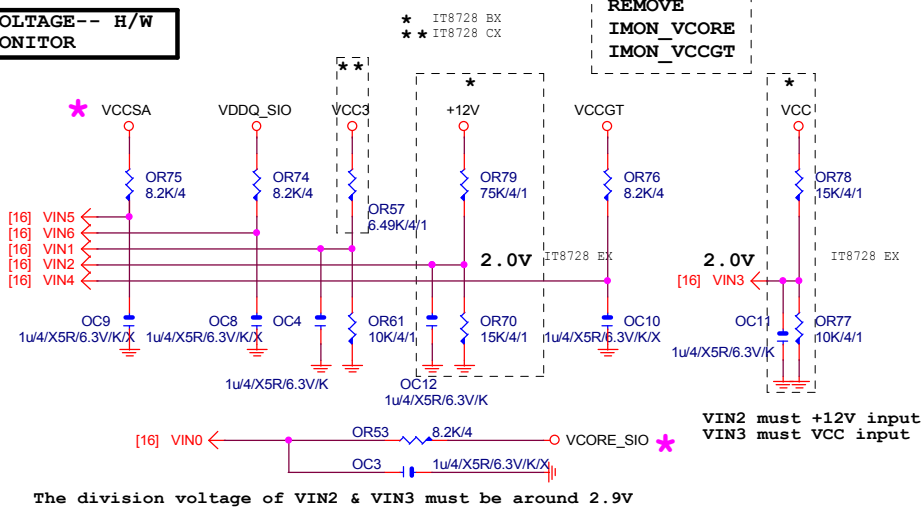
DEBUG PORT



RS_VCORE > RS_VCCGT CLOSE CPU_VCORE & VCCGT MOSFET

~~PROCHOT: 有mos heartsink不用prochot function~~

VOLTAGE-- H/W MONITOR

VIN2 must +12V input
VIN3 must VCC input

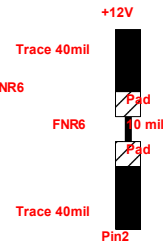
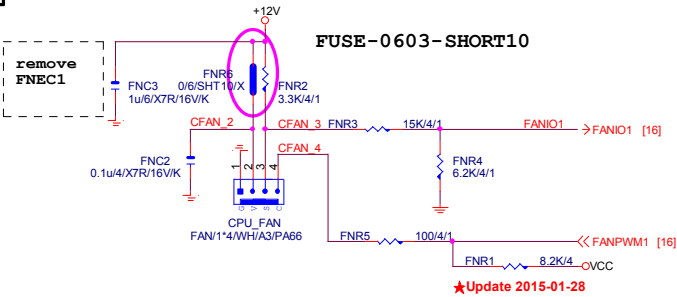
The division voltage of VIN2 & VIN3 must be around 2.9V

Gigabyte Technology

Title			HWM,KB/MS, FAN CTRL		
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Custom					1.0
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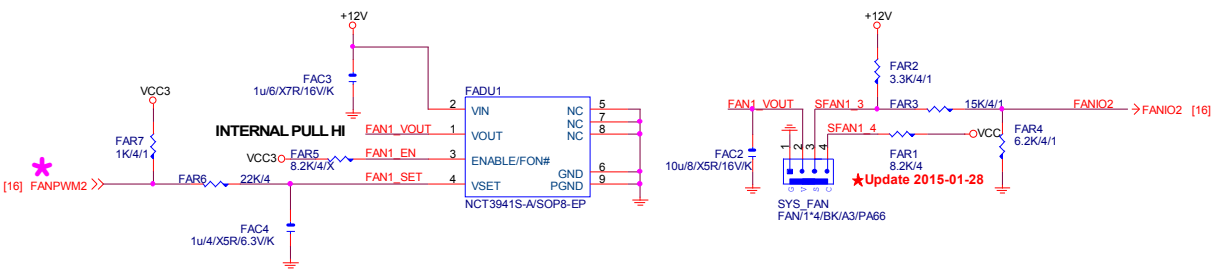
CPU SMART FAN

Rev: 0.61



SYSTEM FAN1

A. Linear SYS_FAN
Enable Function (NCT3941S)
Full Turn On Function (NCT3941S-A)

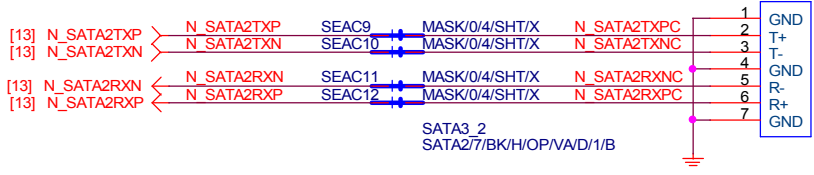
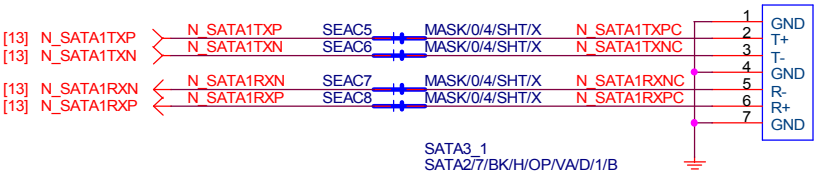
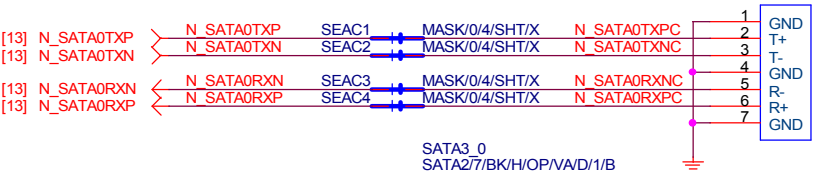


SYSTEM FAN2

N/A

SYSTEM FAN3

N/A



Gigabyte Technology

Title			
SATA			
Size	Document Number		Rev
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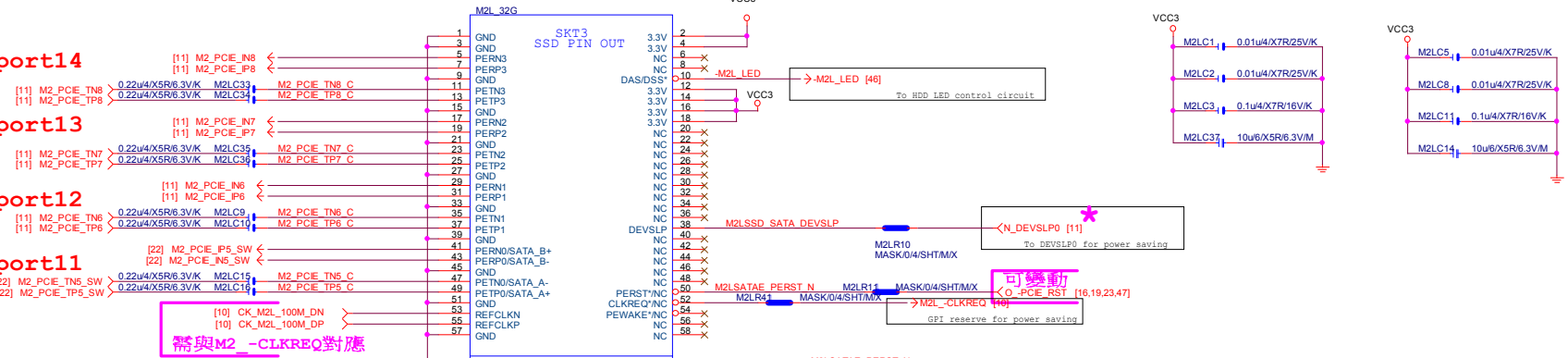
Rev 0.6

M.2 Lane4 from PCH port14

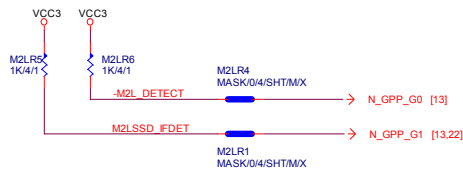
M.2 Lane3 from PCH port13

M.2 Lane2 from PCH port12

M.2 Lane2 from PCH port11



支援SATA and M.2 function



需與M2_-CLKREQ對應

```
NGFF-M-75P-CUT42
REMOVE 42A, FOOTPRINT正反共用.
H110's PCIE is Gen2.
```

SATA 與 PCIE 切換 with switch

	N_GPP_G1
PCIE	1
SATA	0

DIP螺柱

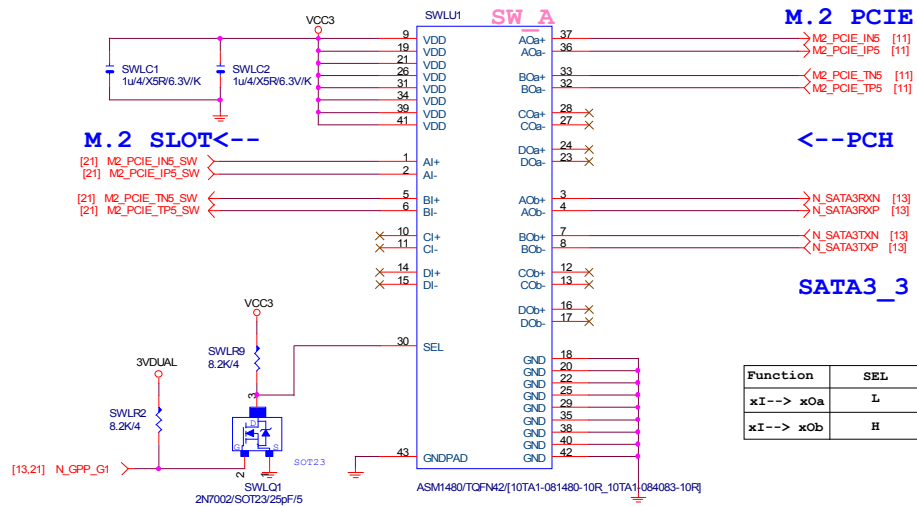
DIP螺絲

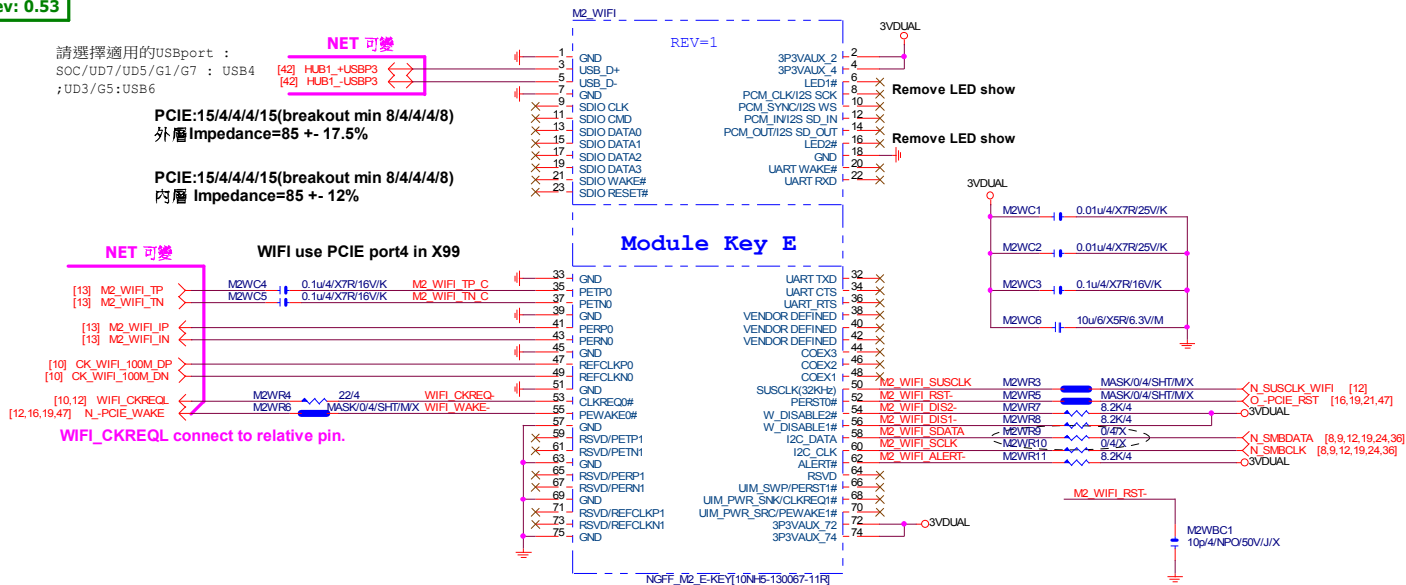
SMD螺柱

FOOTPRINT:276c236B165P

M.2 上在背板須修改:

1. DIP 螺絲背板上件
2. DIP 螺柱背板上件, 須修改料號
3. SMD 螺柱正面上件, 須修改料號及 FOOTPRINT 正反共用.





FOR M.2 WIFI MODULE ON BOARD

WIFI CARD 螺絲BOM 建成WIFI-BRACKET

WIFI-SCREW



SCREW M2*4mm/[12KS2-010204-31R]/X

N/A-->已包含在WIFI-BRACKET内

WIFI-CAP



M2_WIFI_CAP/[11KWP-000001-11R]/X

白色透明

MODULE 可變

M.2 EKEY

WIFI_MODULE
WI-FI WITH BT M2 CARD QUAL COM/120GB1-028260-10B/X

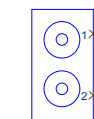
○

ANT2
S-010001-71R/X

Q

ANT1
SMAV[11NH6-010001-71R]/X

ANTENNA BRACKET



VERTICAL
ANTENNA HOLD-5

ANTENNA-BRACKET_Vertical/[12AC2-000001-31R]

WIFI-BRACKET



WIFI-BRACKET/[12AC2-000005-01R]/X

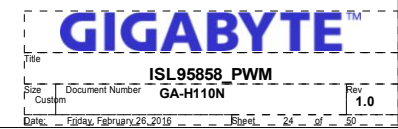
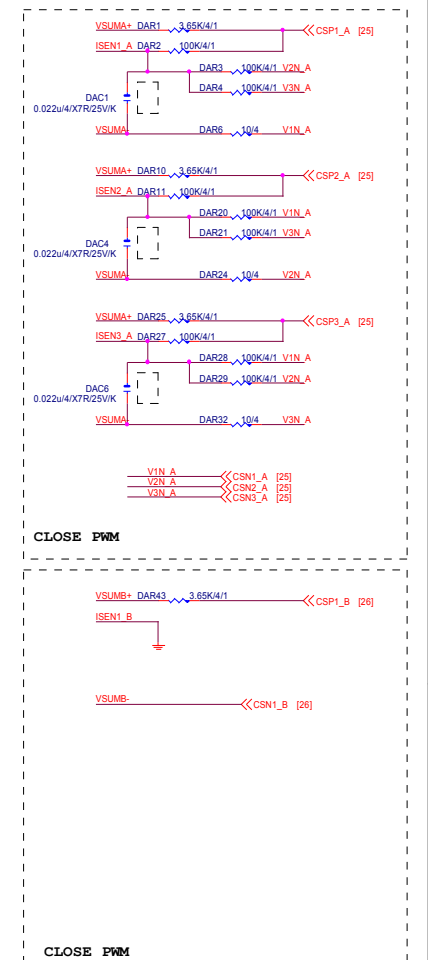
M.2 WIFI支架料號包含
底座螺絲及CARD螺絲

FOOTPRINT:
M2-WIFI-BRACKEY

GIGABYTE™

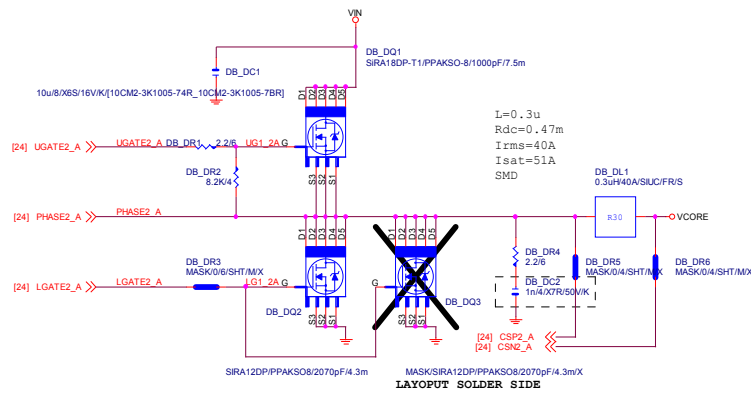
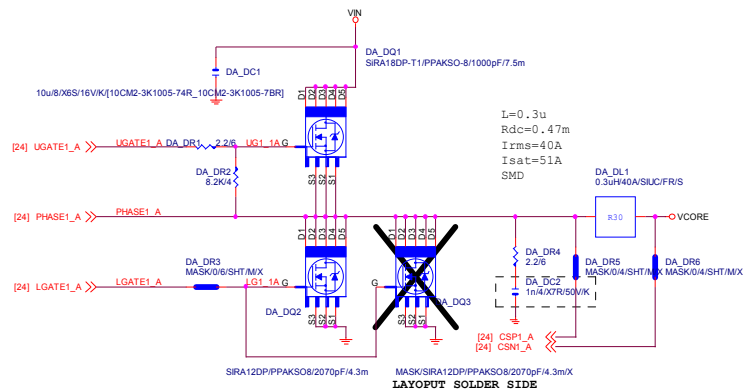
M2_WIFI_E_KEY
GA-H110N

Rev
1.0

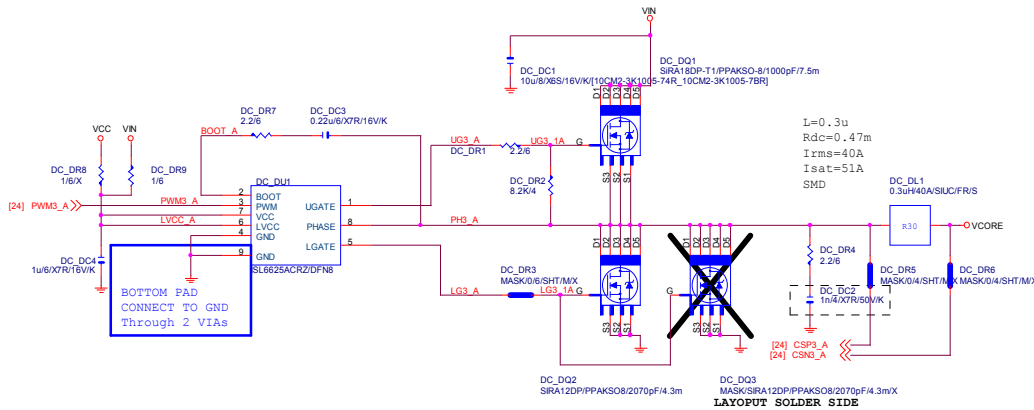
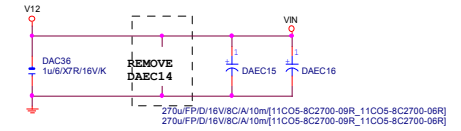


REV:0.9

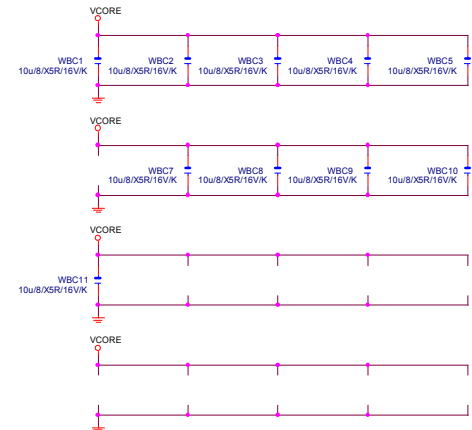
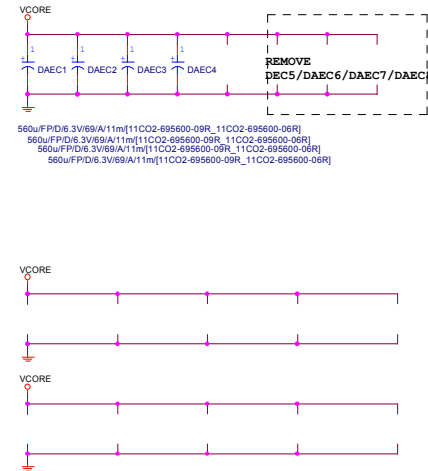
VCORE



VIN CAP 270u*2PCS



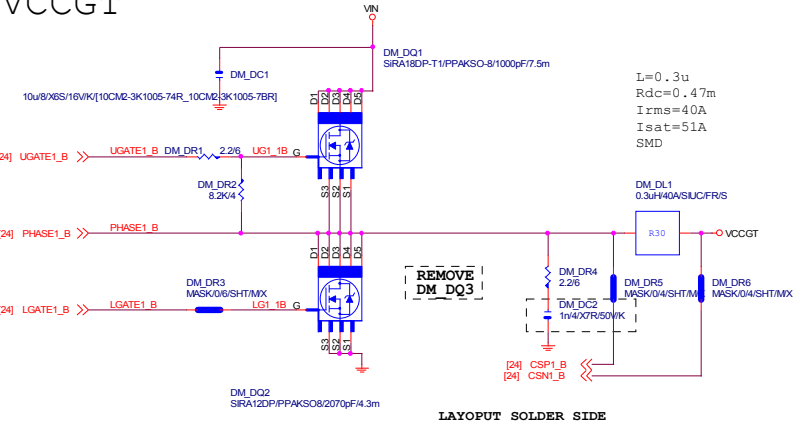
VCORE CAP 560u*4PCS
22u*10PCS



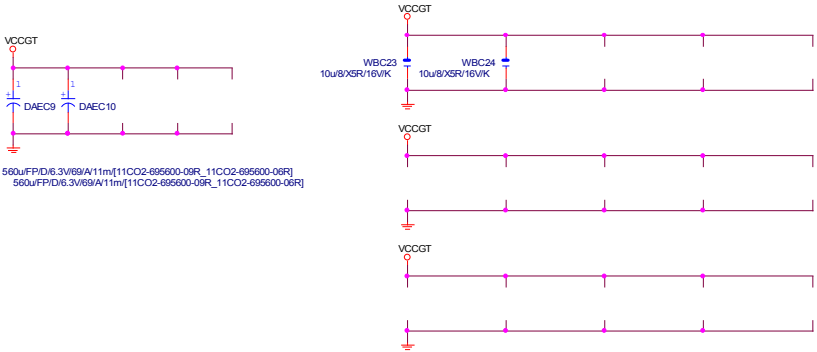
GIGABYTE™

Title ISL95858 MOS
Size Document Number GA-H110N
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VCCGT



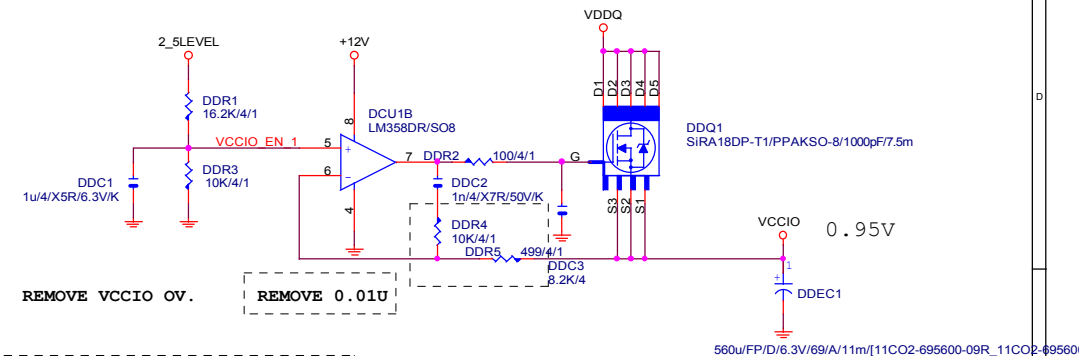
VCCGT CAP 560u*2PCS
22u*2PCS



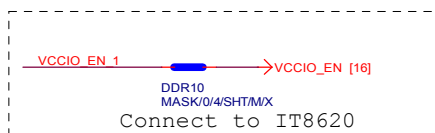
GIGABYTE™

Title ISL95858_MOS
Size Custom Document Number GA-H110N Rev 1.0
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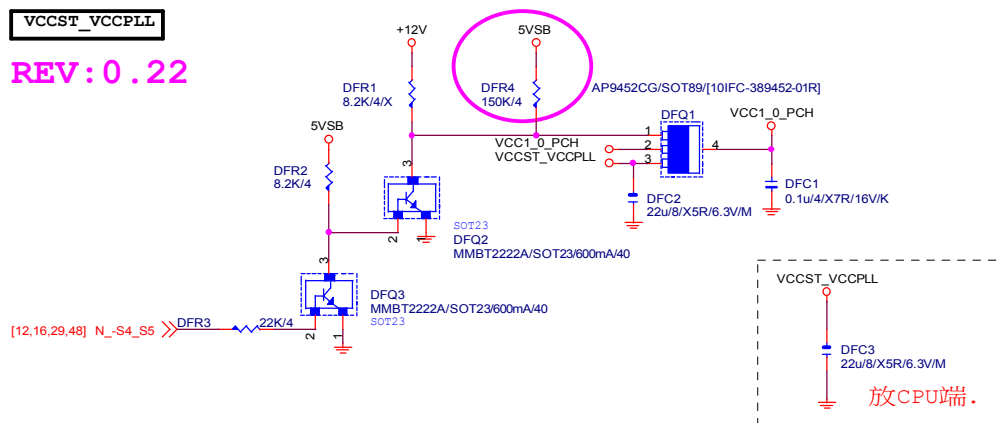
REV: 0.4



REMOVE 0.01U

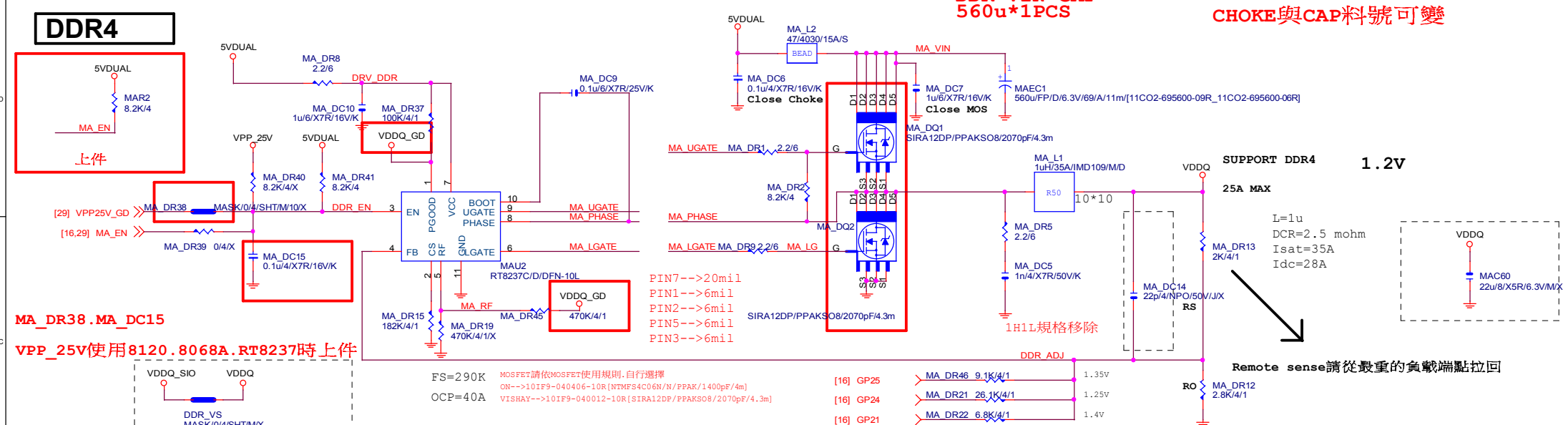


REV: 0.22



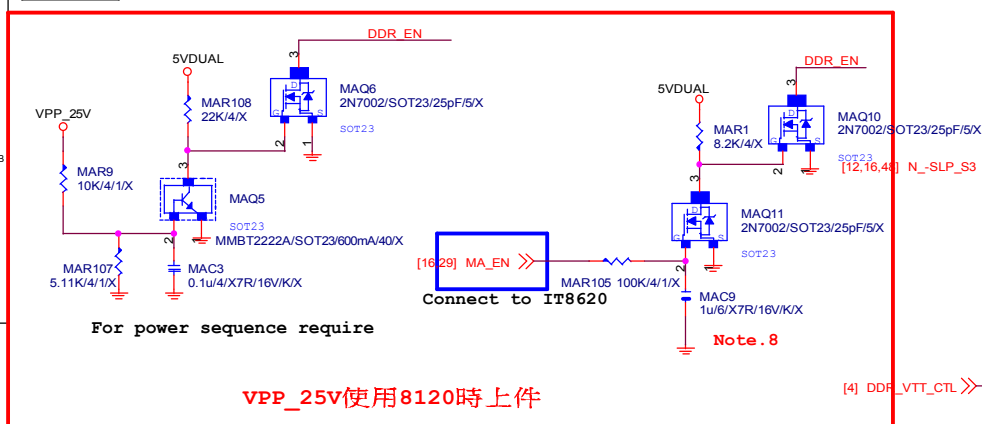
Title				VCCSA VCCIO			
Size	Document Number					Rev	
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DDR4

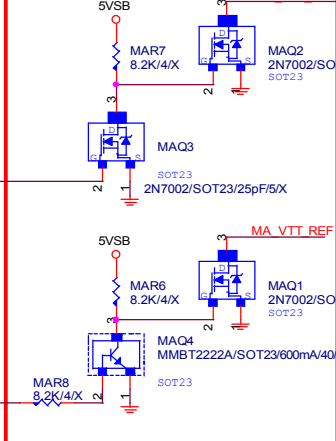


PWR SEQ

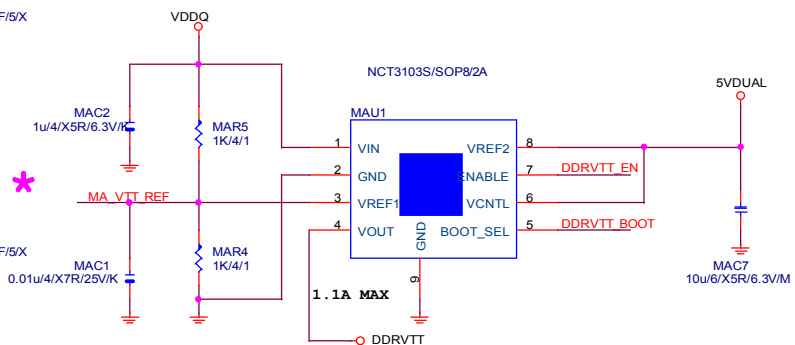
CLOSE TO DDR POWER PLANE



MAU1上RT9045時上件(不可MASK)



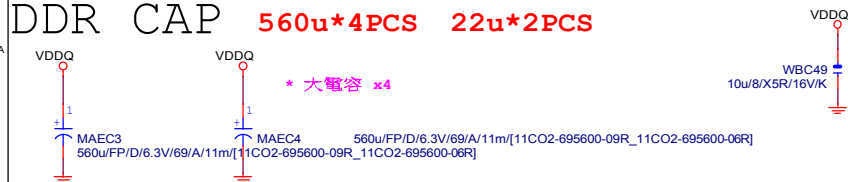
DDRVTT



DDR VTT CTL	MAR110	0/4	DDRVTT EN
N -SLP S3	MAR111	0/4	DDRVTT BOOT

MAU1上NCT3103S時上件(不可以改short pad)

DDR	CAP	560u*4PCS	22u*2PCS
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DDRVTT CAP

**GIGABYTE™**

Title	RT8237 DDR4 POWER
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Custom	GA-H110N

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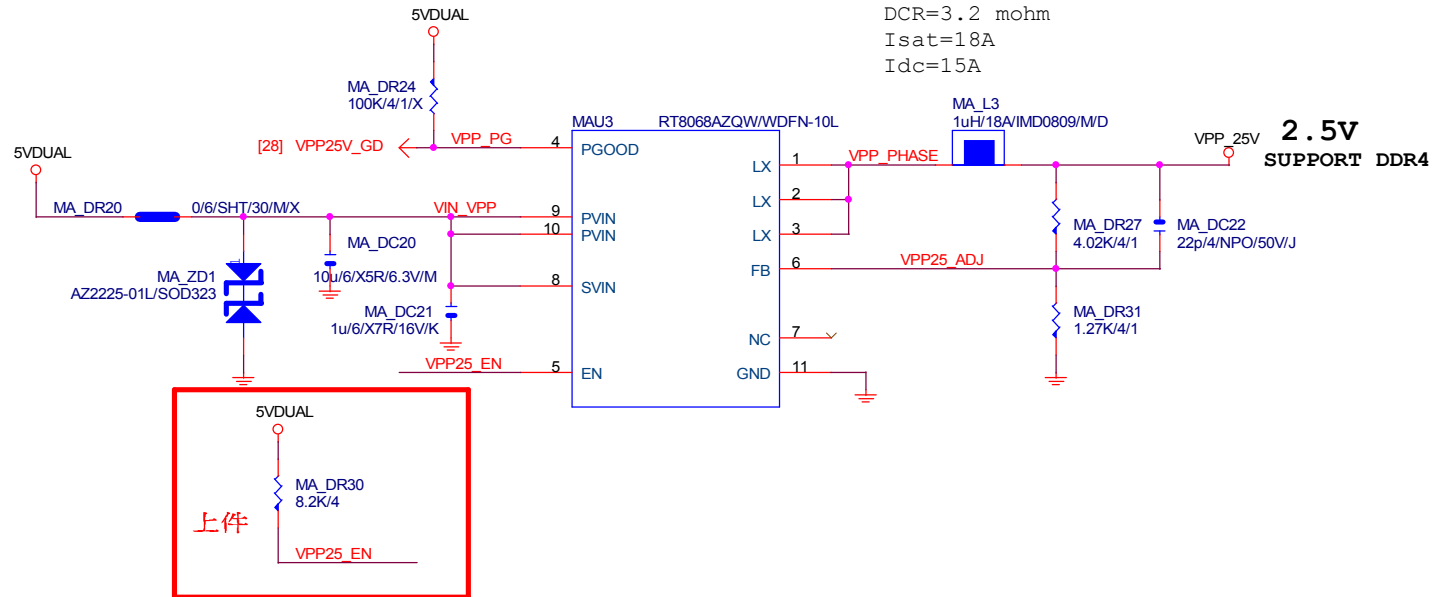
Date: Friday, February 26, 2016 Sheet 28 of 50

REV:0.4

VPP 25V

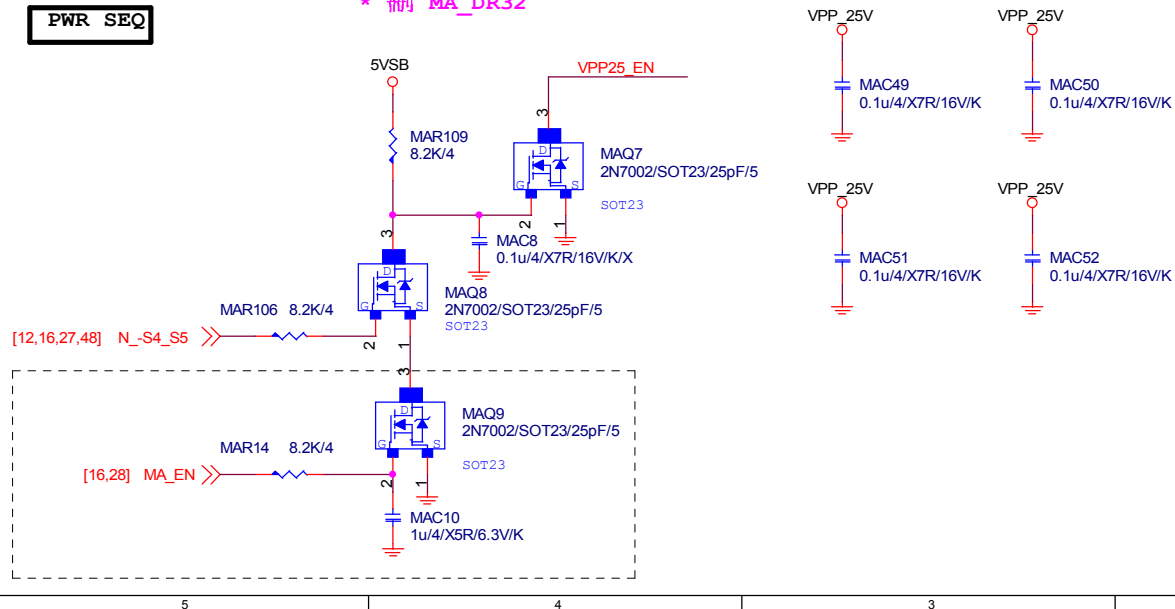
CHOKE與CAP料號可變

L=1u
DCR=3.2 mohm
Isat=18A
Idc=15A



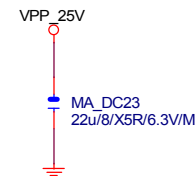
PWR SEQ

* 刪 MA_DR32



VPP CAP 22u*1PCS

* 大電容 x0



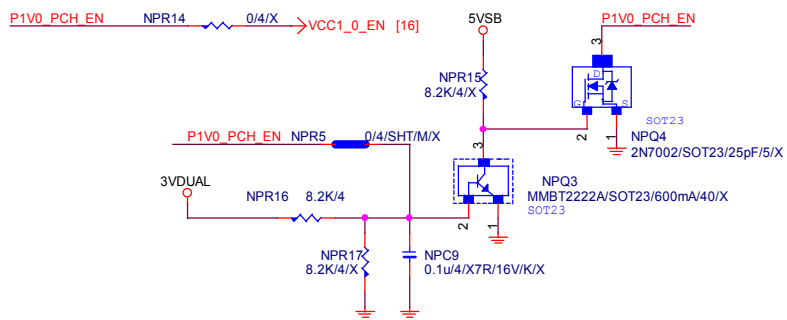
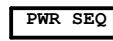
GIGABYTE™

Title
RT8068A_VPP25 POWERSize
Custom Document Number
GA-H110NRev
1.0

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1
+
NPEC1
100u/OS/D/16V/69/A/35m/[11



VCC1_0_PCH

NPC10
22uB/X5R/6.3V/M

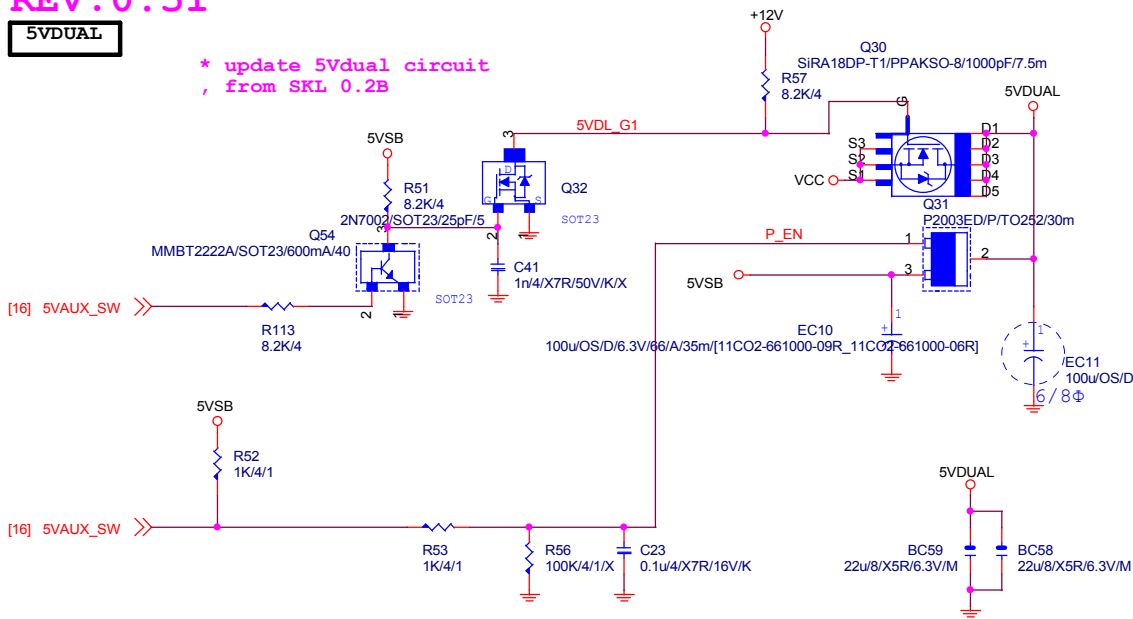
請放置CHOKE一出來的地方

GIGABYTE™			
Title			
RT8237_PCH POWER			
Size Custom	Document Number GA-H110N	Rev 1.0	
Date: Friday, February 26, 2016	Sheet	30	of 50
2		1	

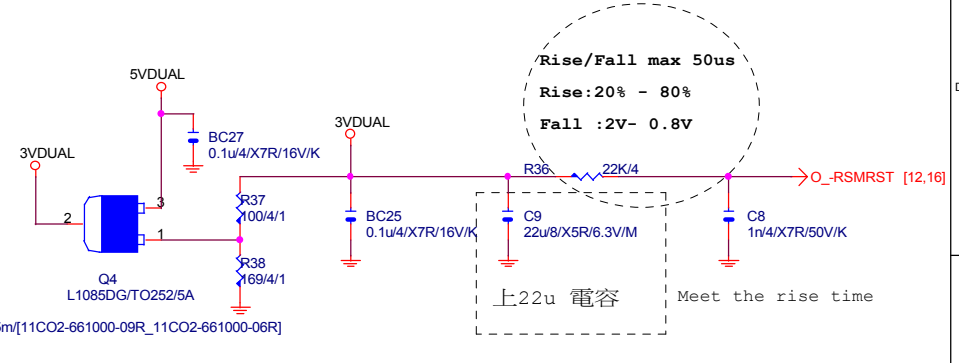
REV:0.51

5VDUAL

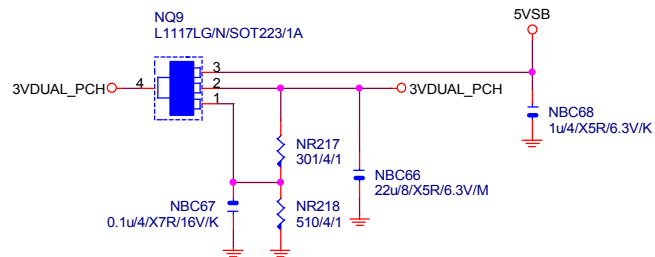
* update 5Vdual circuit
 , from SKL 0.2B



3VDUAL

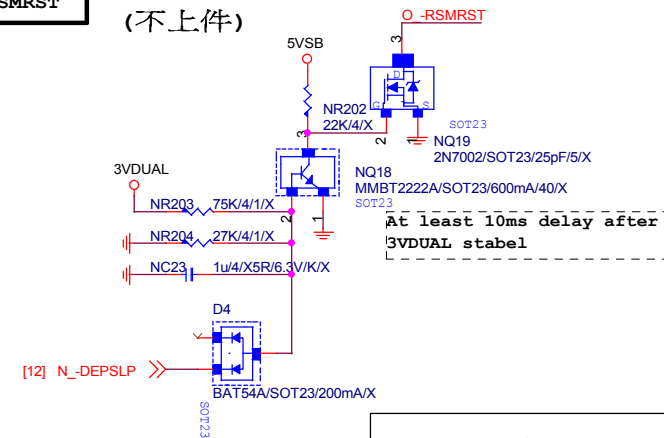


3VDUAL_PCH



O_-RSMRST

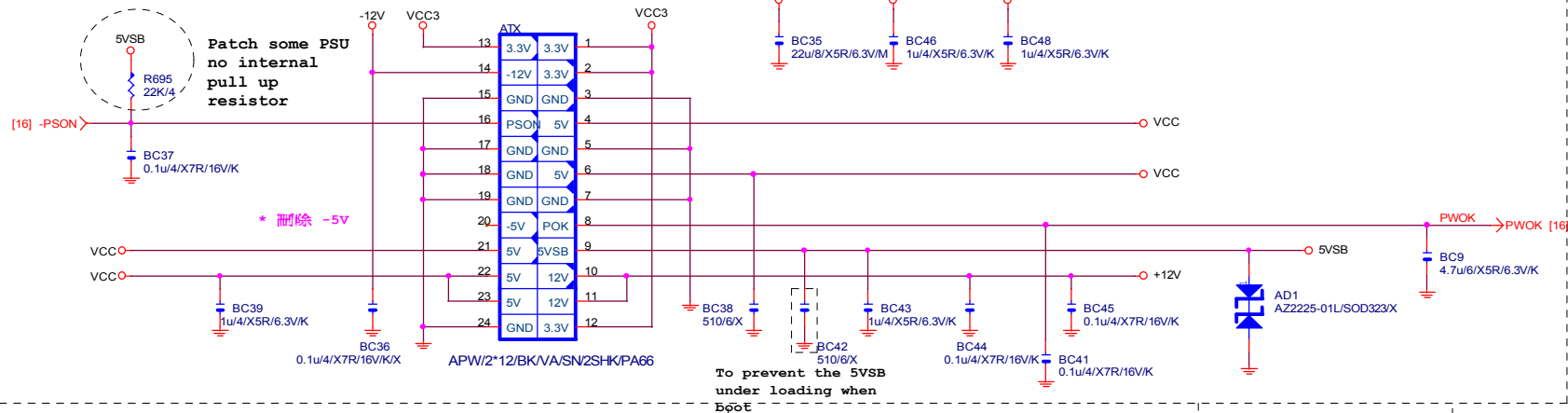
(不上件)



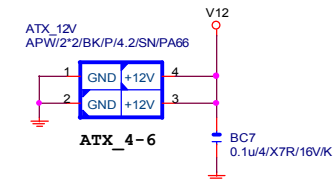
Gigabyte Technology

Title				
DISCRETE POWER				
Size	Document Number			Rev
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ATXX24 POWER CONNECTOR



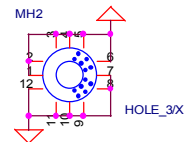
ATXX4 POWER CONNECTOR



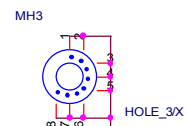
BLACK CONNECTOR

螺絲孔

MH1: GND-T
FOR EMI
TEST驗證

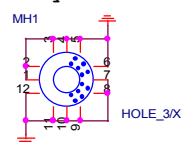


HOLE_4-RH-5MM-1

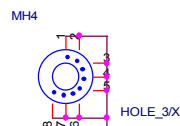


HOLE_4-RH-5MM-5PIN-1

Modify for EMI

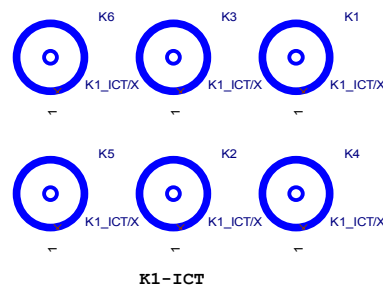


HOLE_4-RH-5MM-1

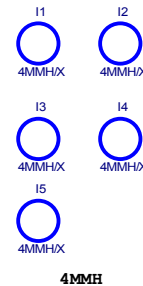


HOLE_4-RH-5MM-5PIN-1

固定孔/光學點

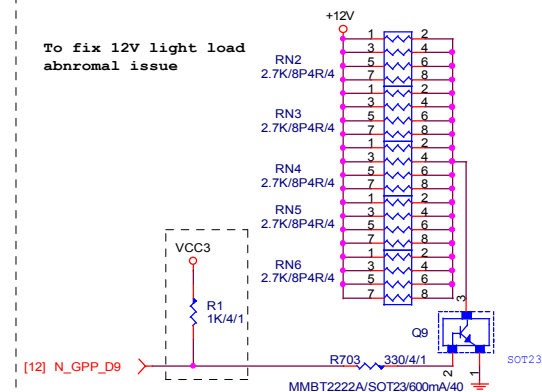


To prevent the 5VSB under loading when boot



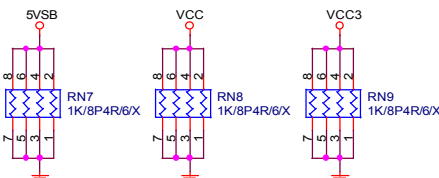
+12V DUMMY LOAD

To fix 12V light load abnormal issue

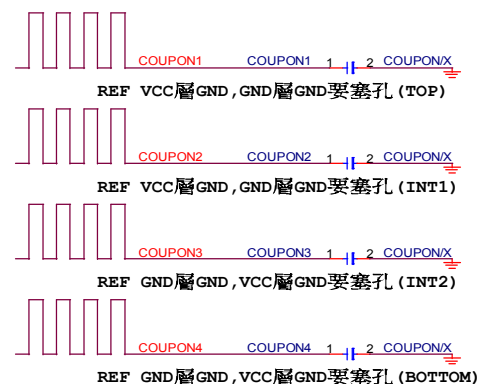


【技術通報R&D技術通報153】

DUMMY LOAD

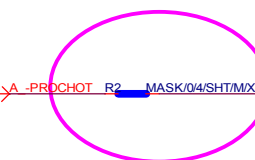


COUPON



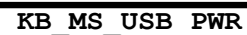
-PROHOT

[4,16] A_PROHOT ← A_PROCHOT R2 MASK/04/SHT/MX → VR_HOT [24]



Gigabyte Technology		
ATX POWER CONNECTOR		
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KB MS USB



AUDIO JACK

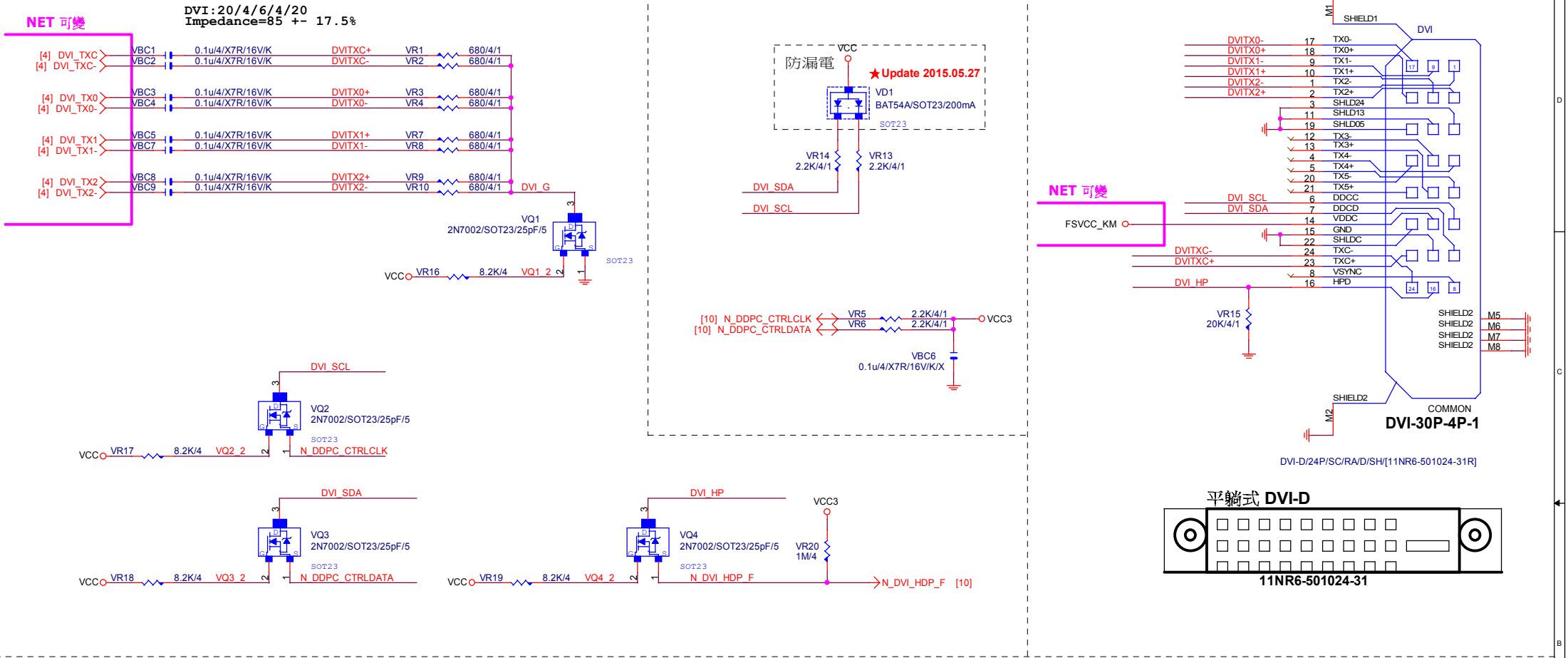
Document Number

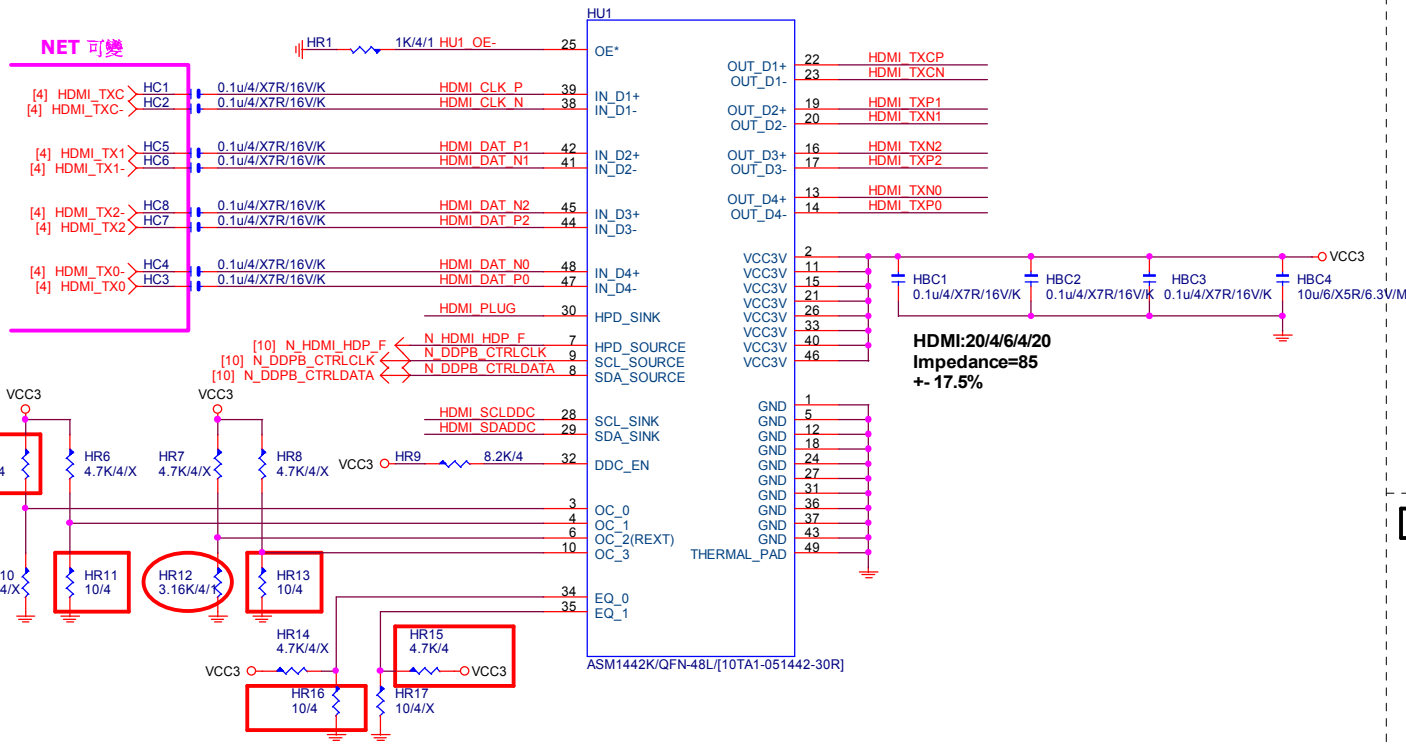
GA-H110N

Rev
1.0

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PTN3360:PIN 4/10/34/35 NC PIN,都不上值;只上HR12:10K

ASM1442:紅色框要上,HR12:3.16K

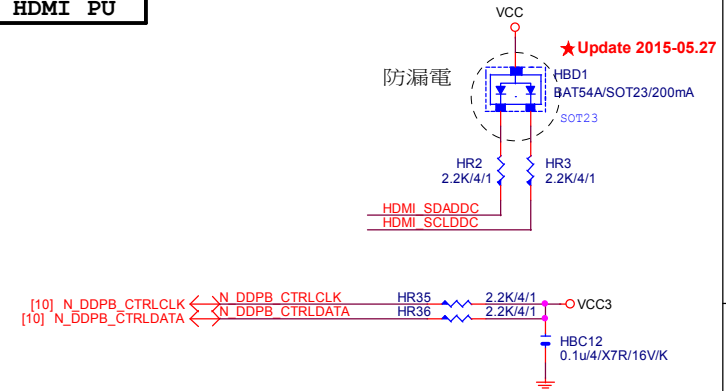
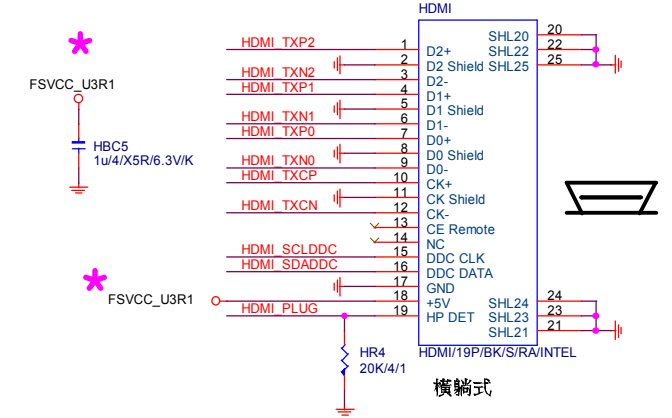
【技術通報R&D技術通報150】

HDMI eye diagram1.4版(deep color)會fail

原因: 因目前的HDMI訊號過長,造成RISING TIME過慢,而會壓到eye diagram

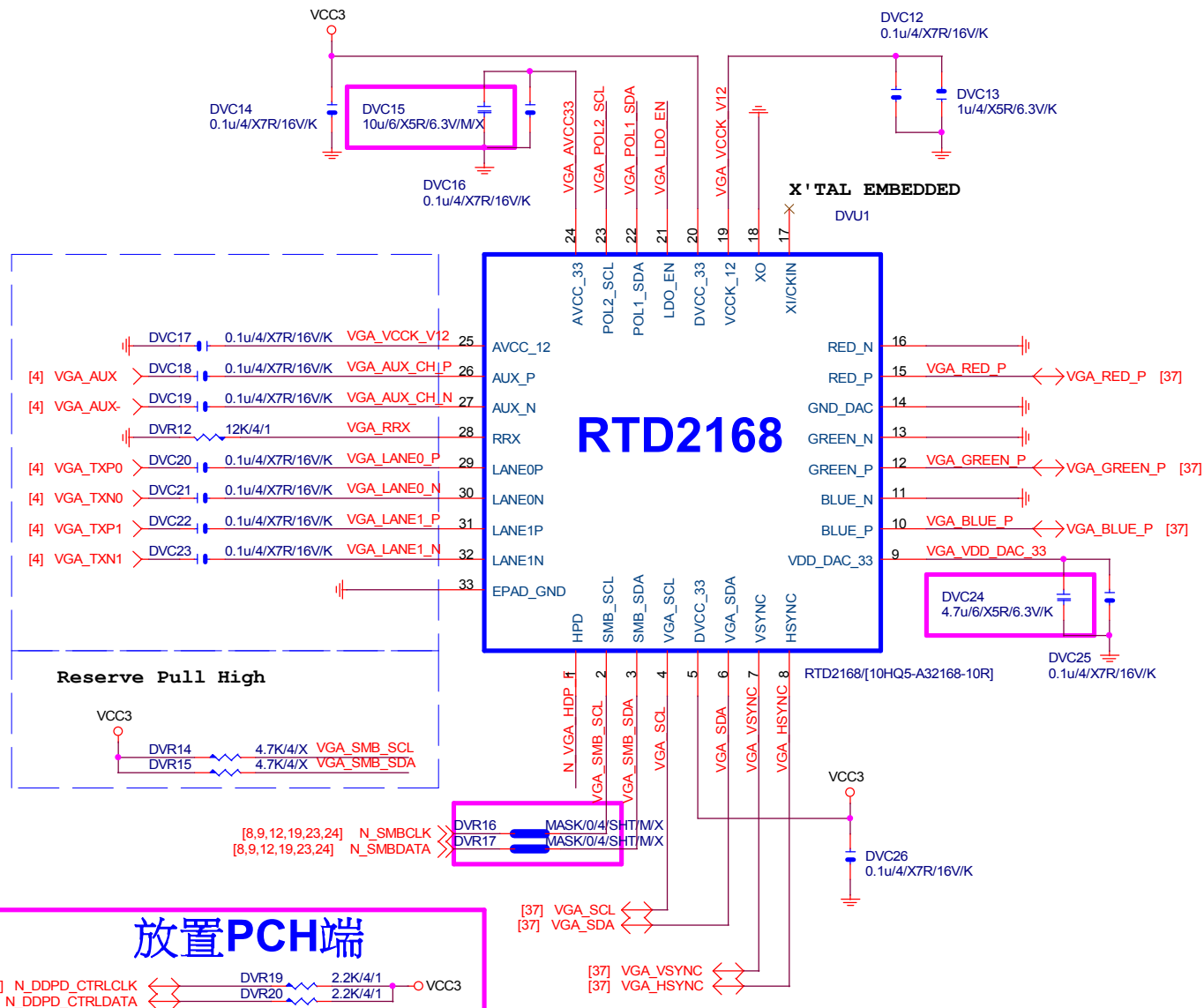
改善: ASMEDIA ASM1442 : 3.16K(PIN6 PULL DOWN電阻) 10ohm(PIN4 PULL

DOWN電阻)



Gigabyte Technology

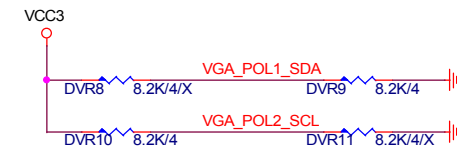
Title			
FP,F_USB,USB PWR,BZ			
GA-H110N			
Size	Document Number	Rev	
Custom		1.0	
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POWER

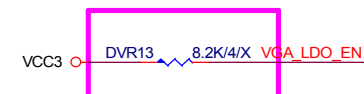


Power on latch



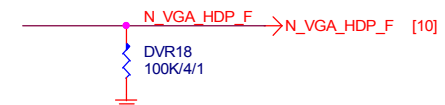
		POL1_SDA(PIN22)	
		0	1
POL2_SCL (PIN23)	0	X	EPROM MODE
	1	ROM ONLY MODE	EEPROM MODE

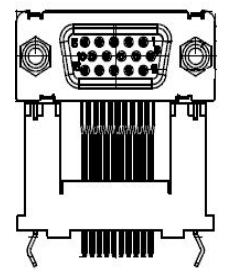
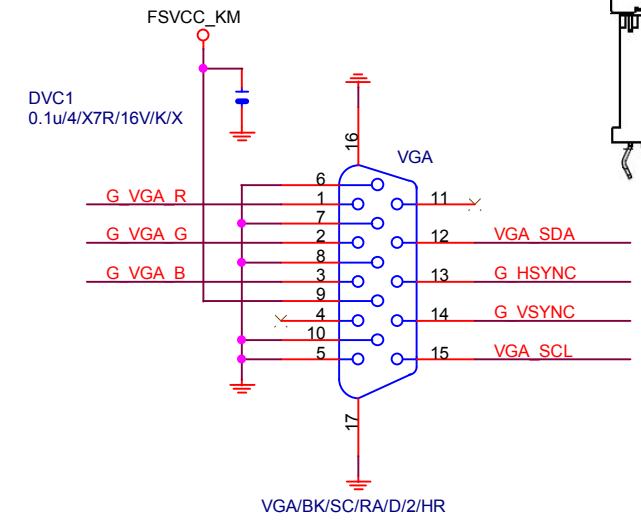
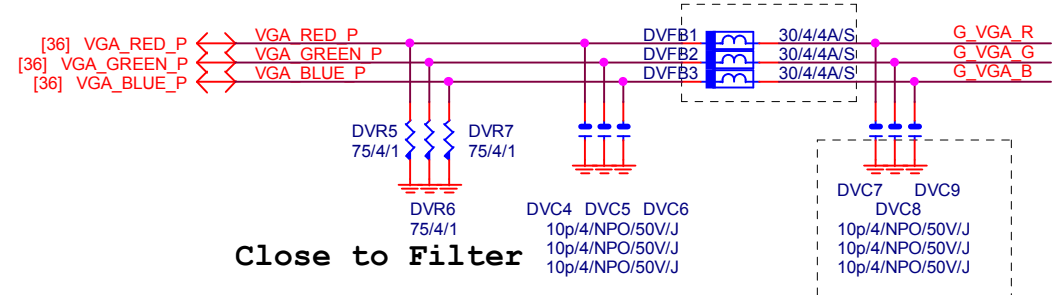
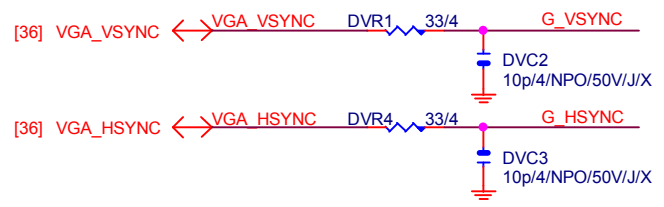
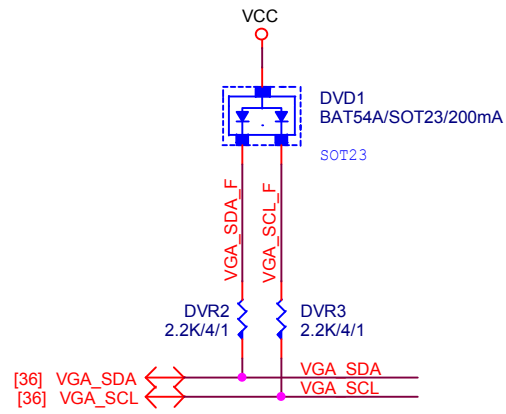
Embedded LDO



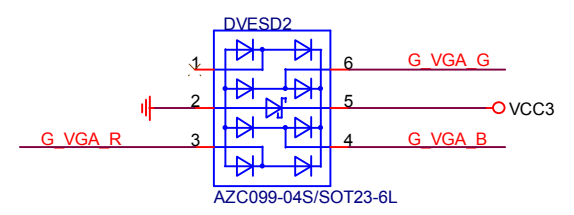
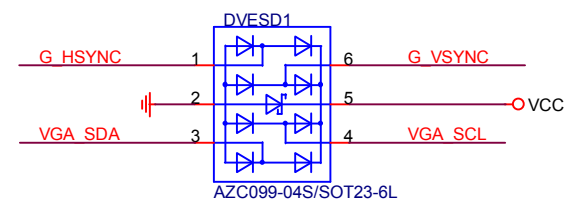
LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

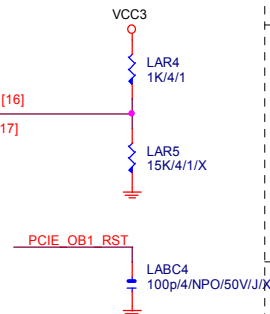
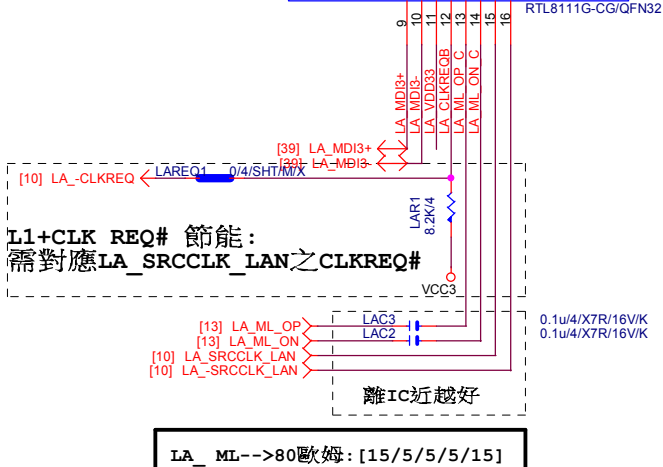
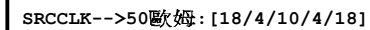
DP HPD



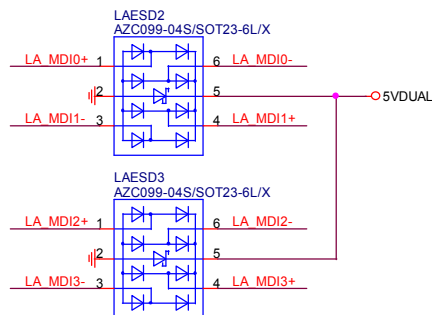


VGA ESD





MDI ESD預留



(CLOSE LAU1 PIN22,30,3,8)

LA_VDD10

Pin22
LABC2
1uF/4X5R/6.3V/K

Pin30
LABC9
0.1uF/4X7R/16V/K

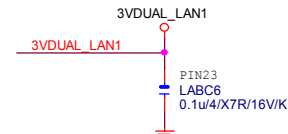
Pin3
LABC3
0.1uF/4X7R/16V/K

Pin8
LABC8
0.1uF/4X7R/16V/K

LA_VDD10

```
LABC2:1U CLOSE PIN22[REALTEK REQ]
```

note: lan power 連接及電流



(CLOSE LAU1 PIN23)

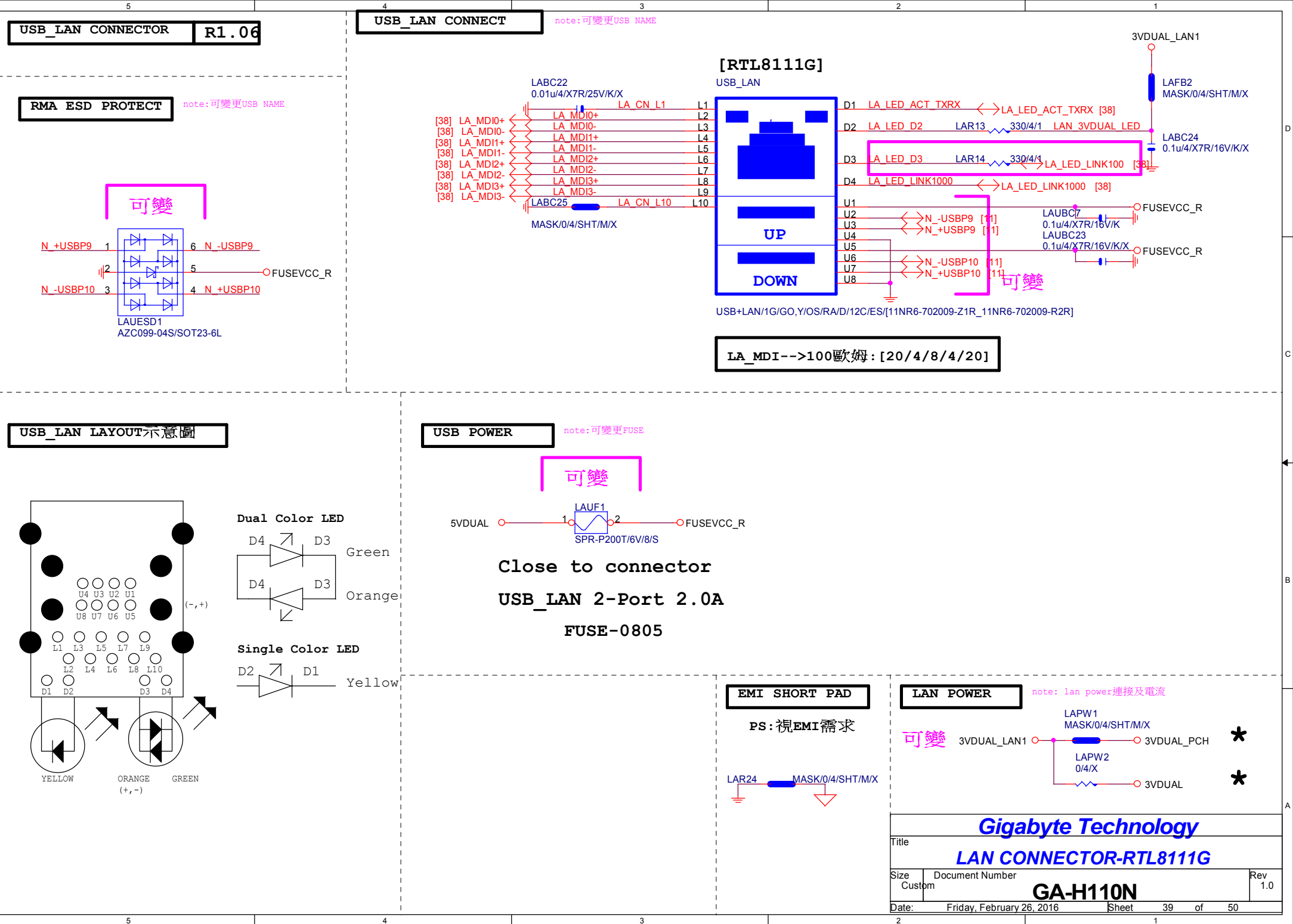
```
LABC18,27:CLOSE PIN11[REALTEK SURGE]
```

LABC14,20:CLOSE PIN32[REALTEK SURGE]

The schematic shows a dashed box representing the LAU1 component. Inside the box, there is a pin labeled LA_REGOUT PIN24 connected to a blue capacitor labeled LABC5 with a value of 0.1µ4/X7R/16V/K. The output of this network is connected to a node labeled LAR8. This node is also connected to a red wire labeled LA_DVDD10, which leads to a terminal labeled LA_DVDD10.

(CLOSE LAU1 PIN24)

<i>Gigabyte Technology</i>			
Title			
<i>Realtek RTL8111GUS</i>			
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USB_LAN LAYOUT示意圖

USB POWER

note:可變更FUSE

可變

Close to connector

USB_LAN 2-Port 2.0A

FUSE-0805

EMI SHORT PAD

PS:視EMI需求

LAN POWER

note:lan power連接及電流

可變

Gigabyte Technology

LAN CONNECTOR-RTL8111G

GA-H110N

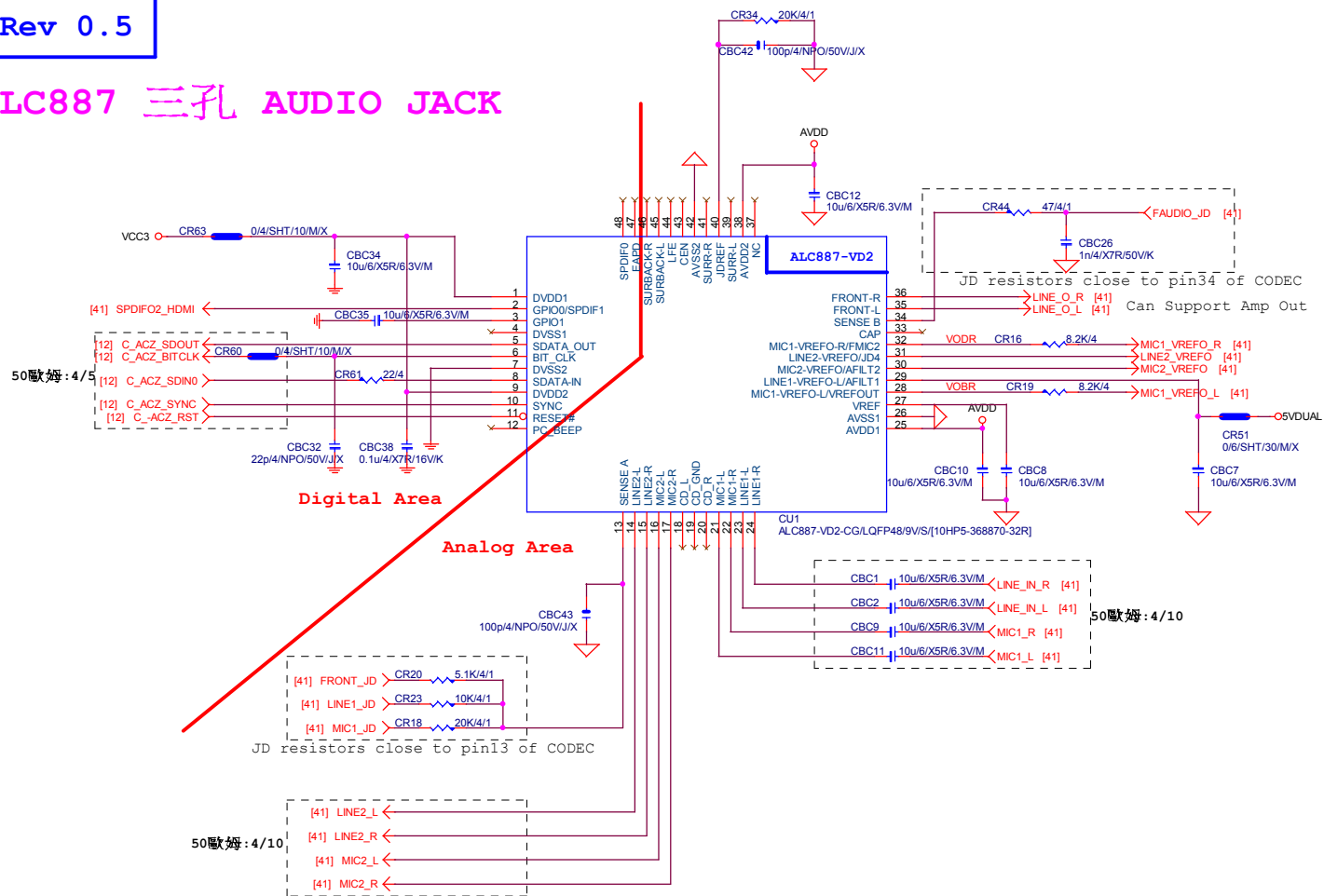
Rev 1.0

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ALC887 三孔 AUDIO JACK



LAYOUT注意: 螺絲孔下GND方式

1. MH1空間夠, 下DGND
空間不夠, 改為Isolate
2. MH2一律改為Isolate

○ MH1	MH2 ○
DGND	Isolate

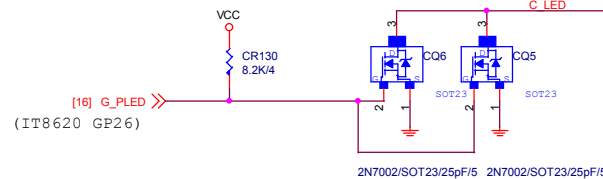
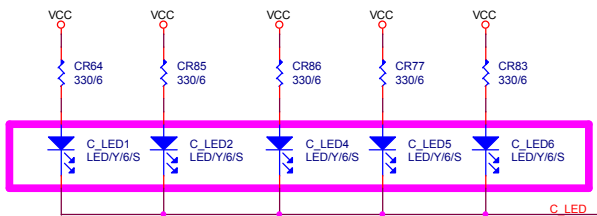
LAYOUT注意: 要加

GND切割線

音效區域印刷



VALUE可變, LED顏色請自行修改
(預設: 低亮度黃色LED: LED/Y/6/S)



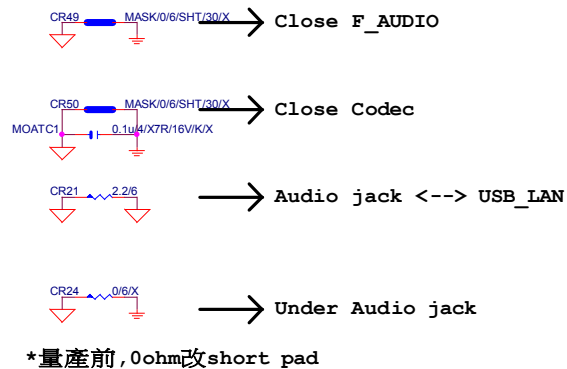
BOM OPTION : 1. Chemicon音效電容
2. 金屬外罩 Reserve (上件與否, 依照各Model spec)
3. LED Reserve (上件與否和LED顏色, 依照各Model spec)

Gigabyte Technology

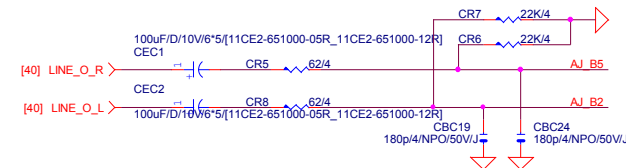
Title HD AUDIO ALC887

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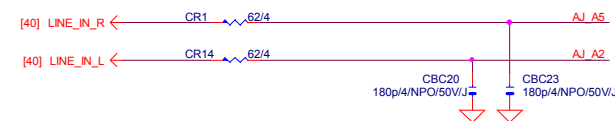
Rev 0.5



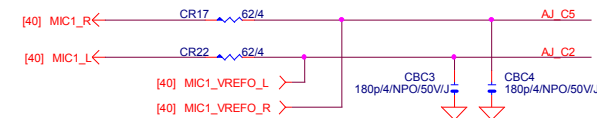
LINE-OUT



LINE-IN



MIC-IN

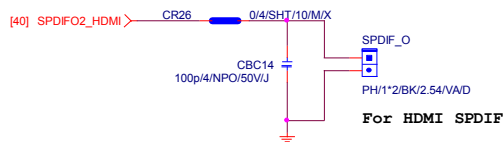


SURROUND

CENLFE

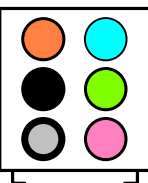
SURRBACK

SPDIF_OUT

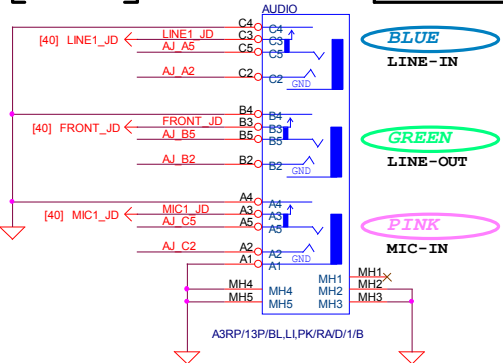


SPDIF_IN

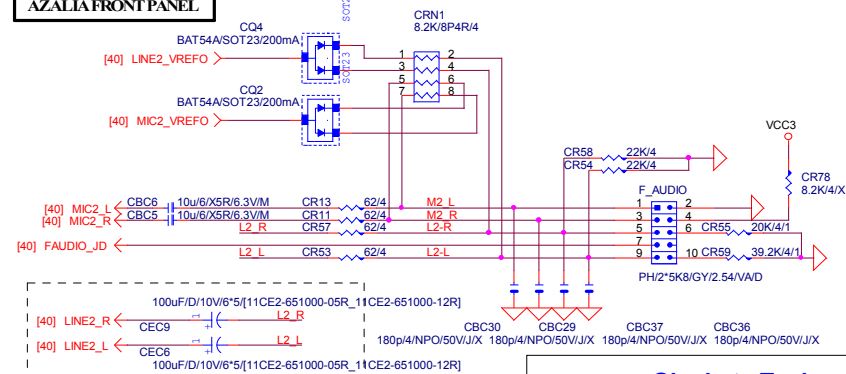
AZALIA JACK



AZALIA JACK

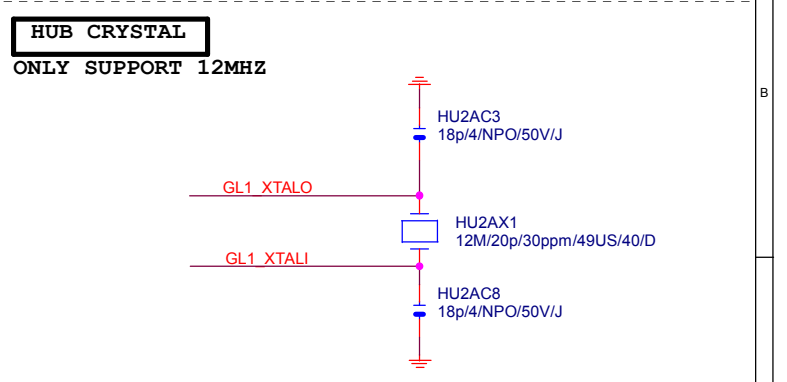
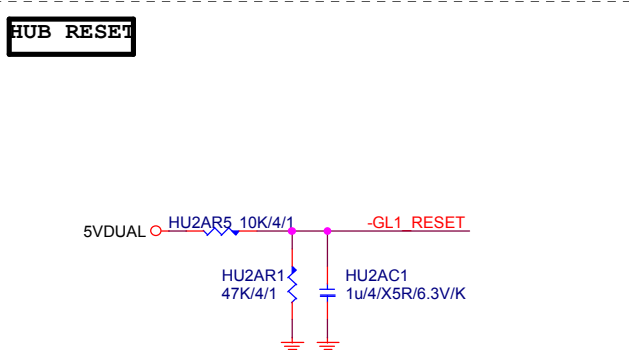
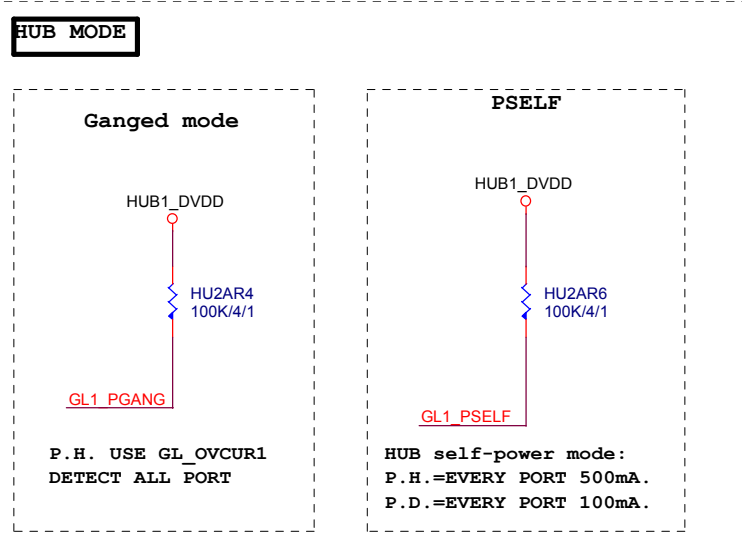
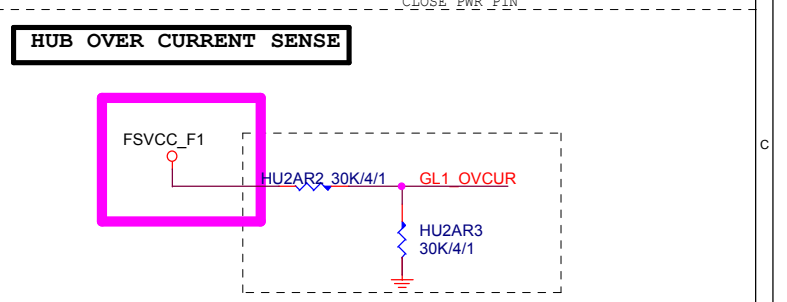
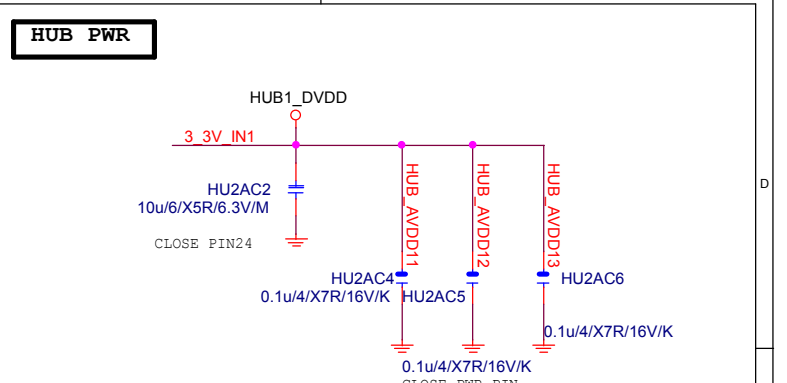
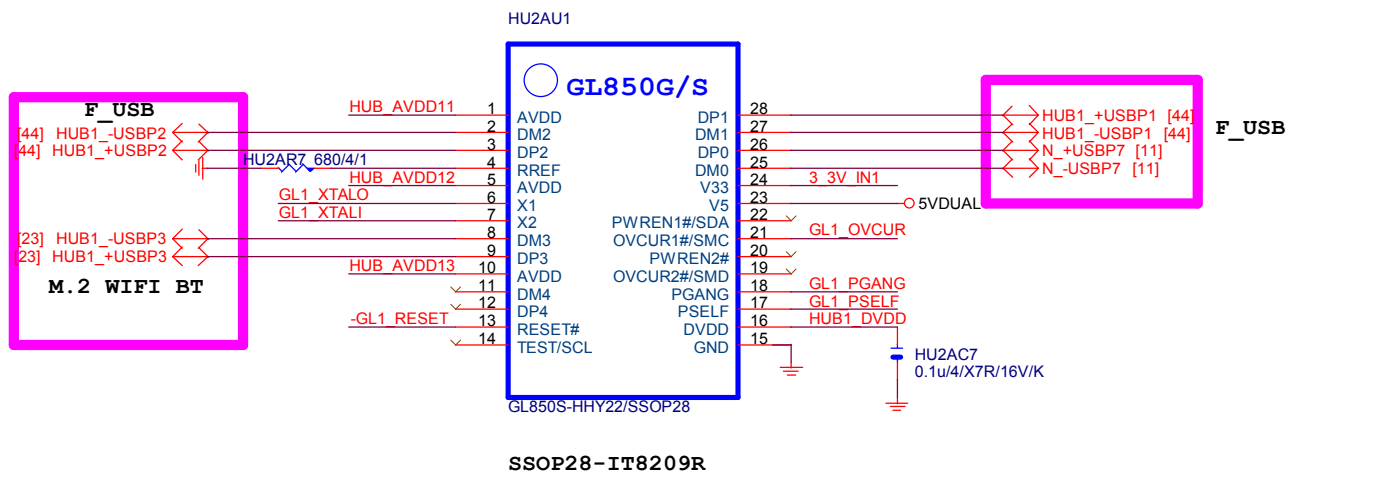


AZALIA FRONT PANEL

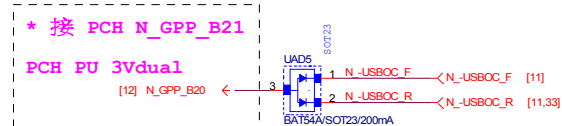
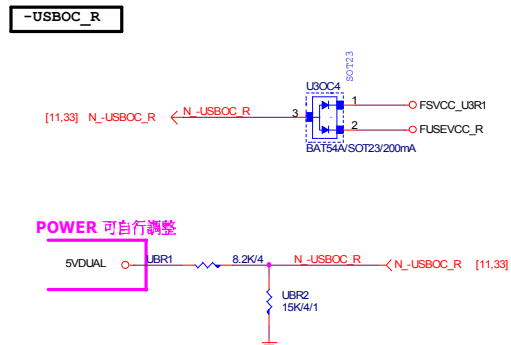
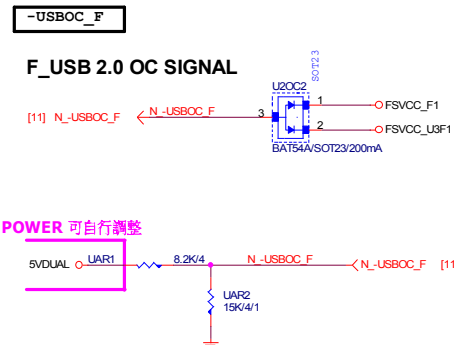
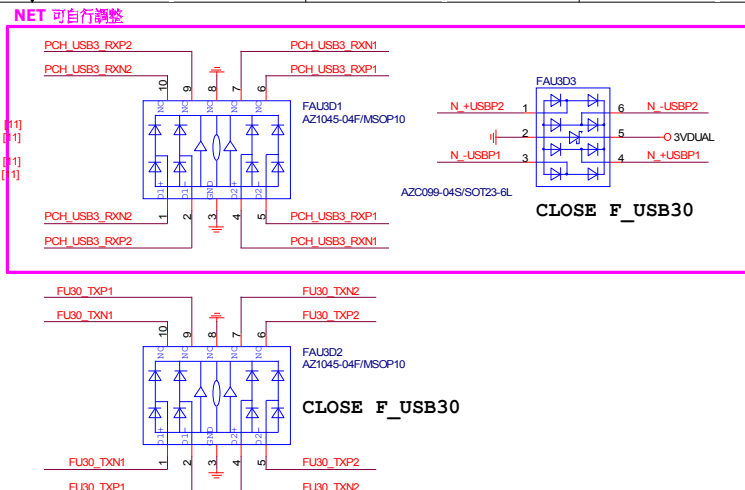
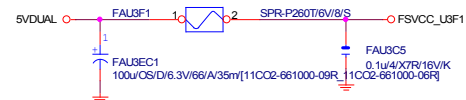


Gigabyte Technology

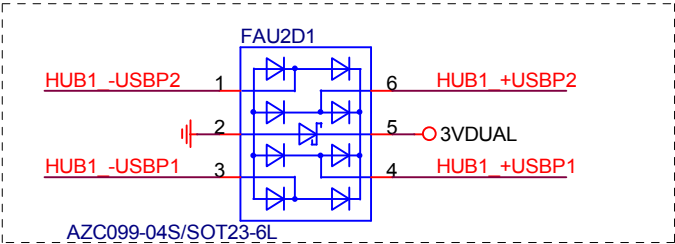
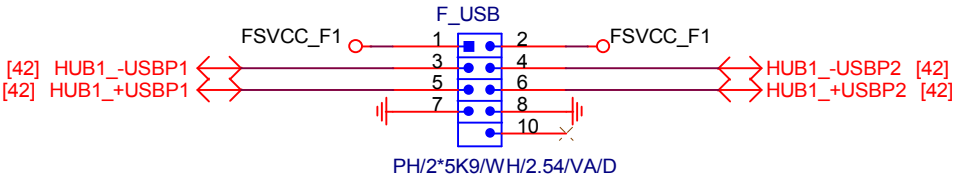
Title				Rev 1.0
AUDIO JACK				
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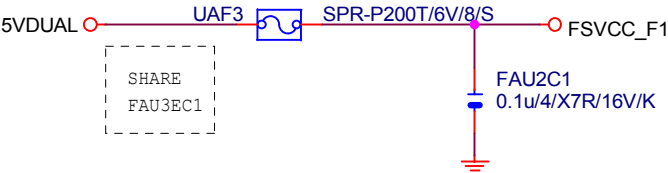
Gigabyte Technology			
Title			
HUB GL850GS_1			
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Custom	GA-H110N	1.0	
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NET 可變



Close to connector
FUSE 2 Port 1 Fuse 2A



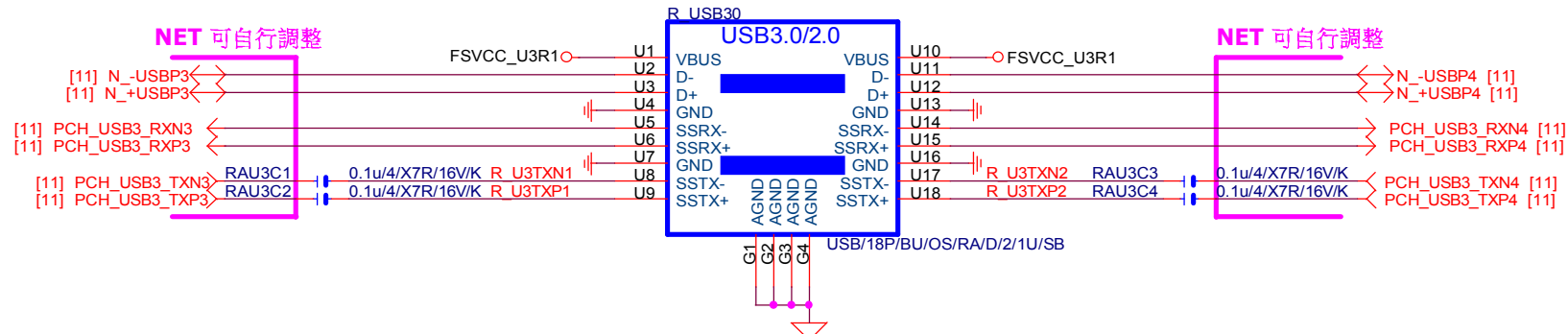
F_USB 2.0 OC SIGNAL-->SCH IN F_USB30
PAGE

Gigabyte Technology

Title			USB2.0		
Size A	Document Number				Rev
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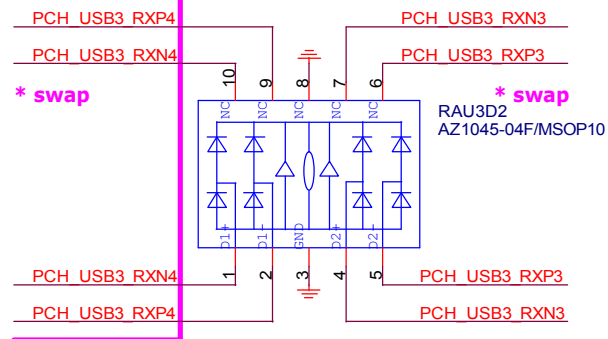
Rev: 0.7

ESD 可自行SWAP PIN ,CONN端 NET 名稱 不可

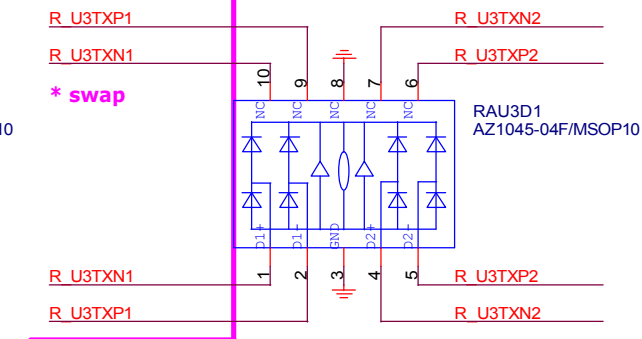


ESD

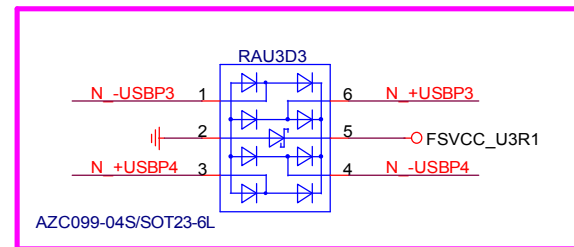
NET 可自行調整



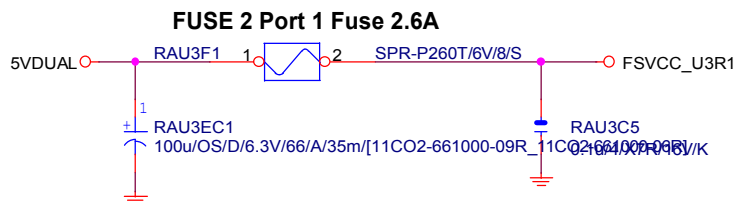
NET 可自行調整



NET 可自行調整



FUSE



Gigabyte Technology

Title

R_USB30,USB_OC

Size Custom

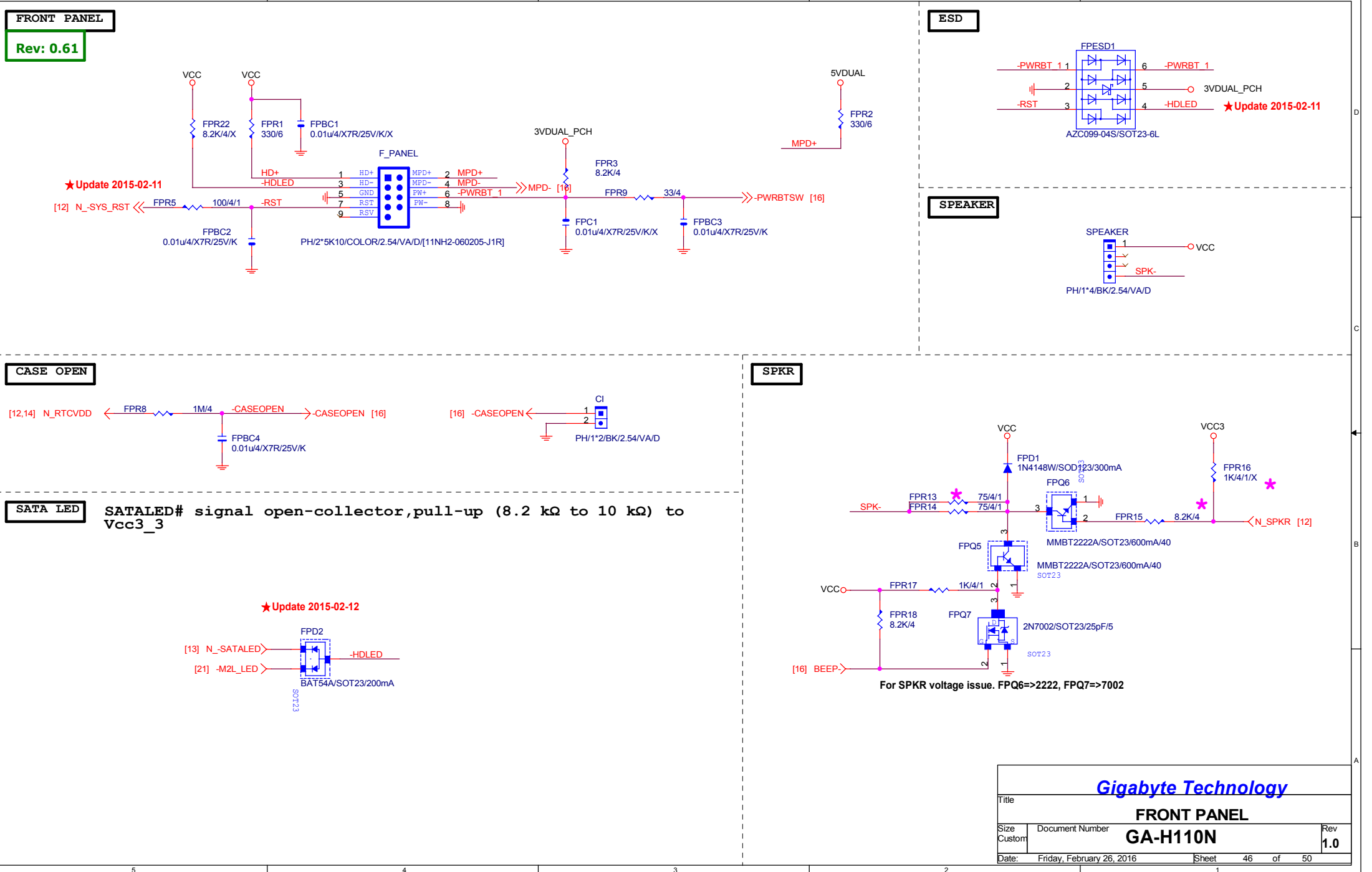
Document Number

GA-H110N

Rev 1.0

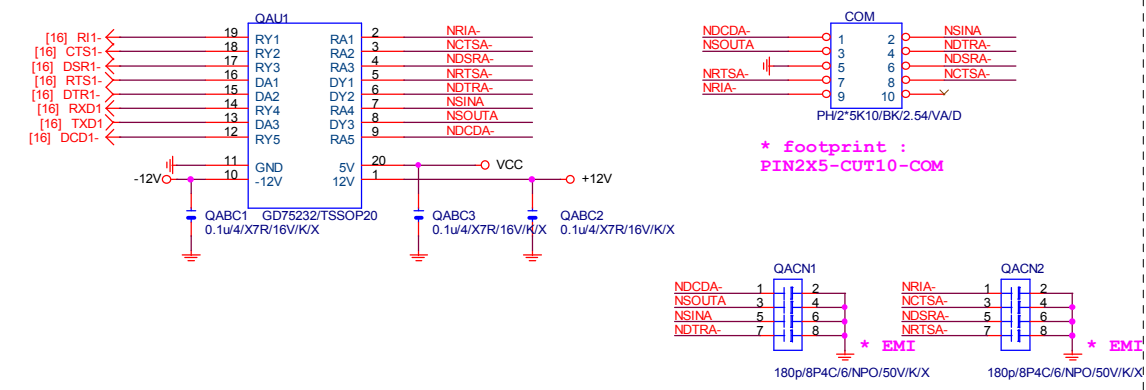
Date: Friday, February 26, 2016

Sheet 45 of 50

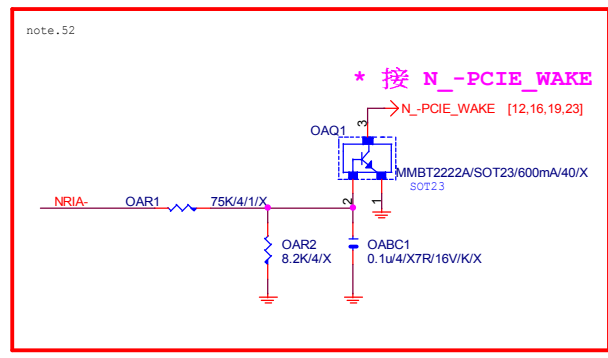


COM PORT

Rev: 0.7



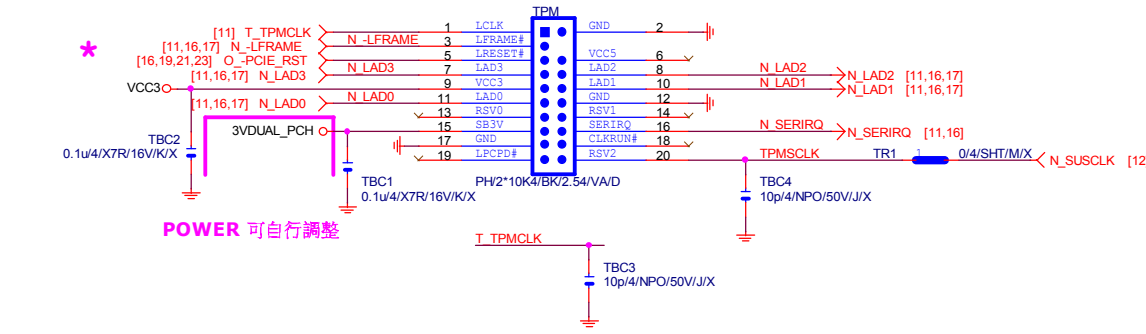
COM RI



LPT PORT

(N/A)

TPM CONNECT



Thunderbolt

(N/A)

CLOSE SIO

EMIC1
100p/4/NPO/50V/J/X

[12,16,28] N_SLP_S3 <—

EMIC2
100p/4/NPO/50V/J/X

[12,16,27,29] N_S4_S5 <—

EMIC3
100p/4/NPO/50V/J/X

[4,12,16] N_CPUPWROK <—

CLOSE PCH

EMIC4
100p/4/NPO/50V/J/X

[4,12,16] N_CPUPWROK <—

GIGABYTE™

Title

EMI/ESDSize
A

Document Number

GA-H110N

Rev

1.0

Date:

Friday, February 26, 2016

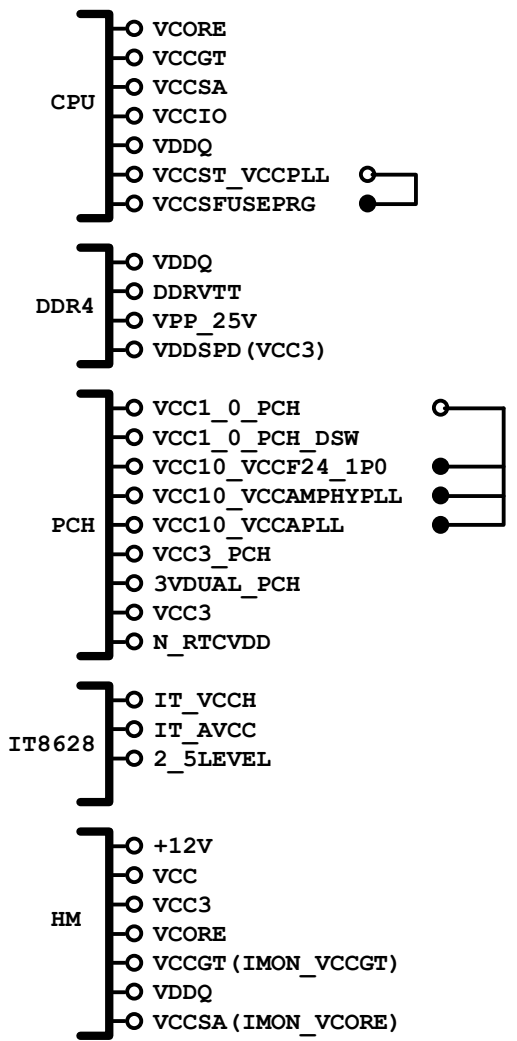
Sheet

48

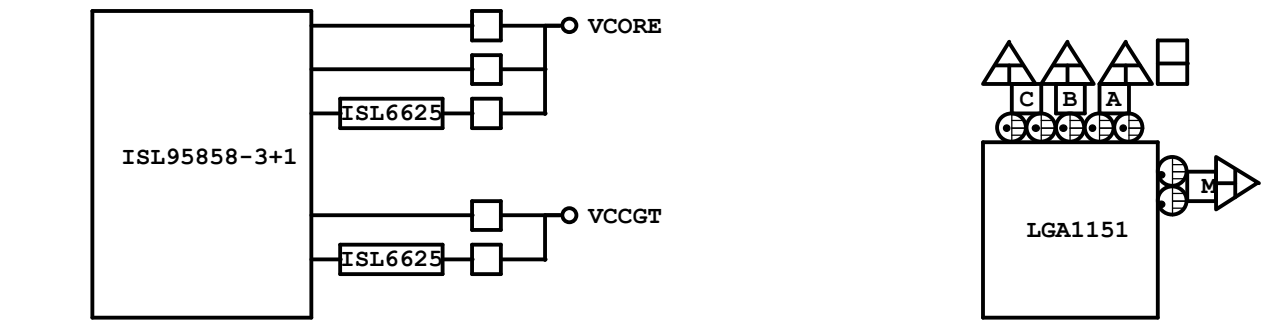
of

50

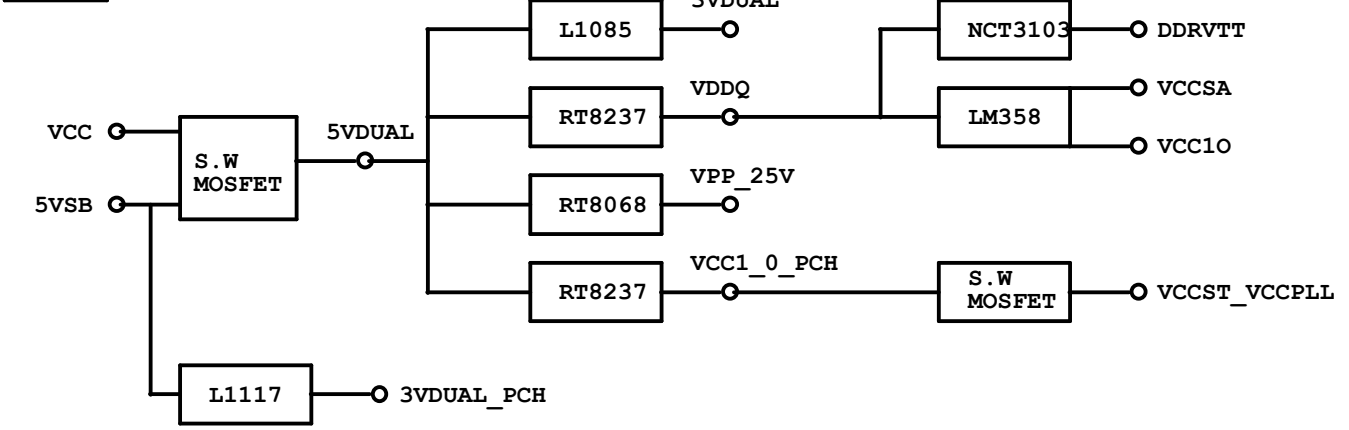
POWER BLOCK MAP



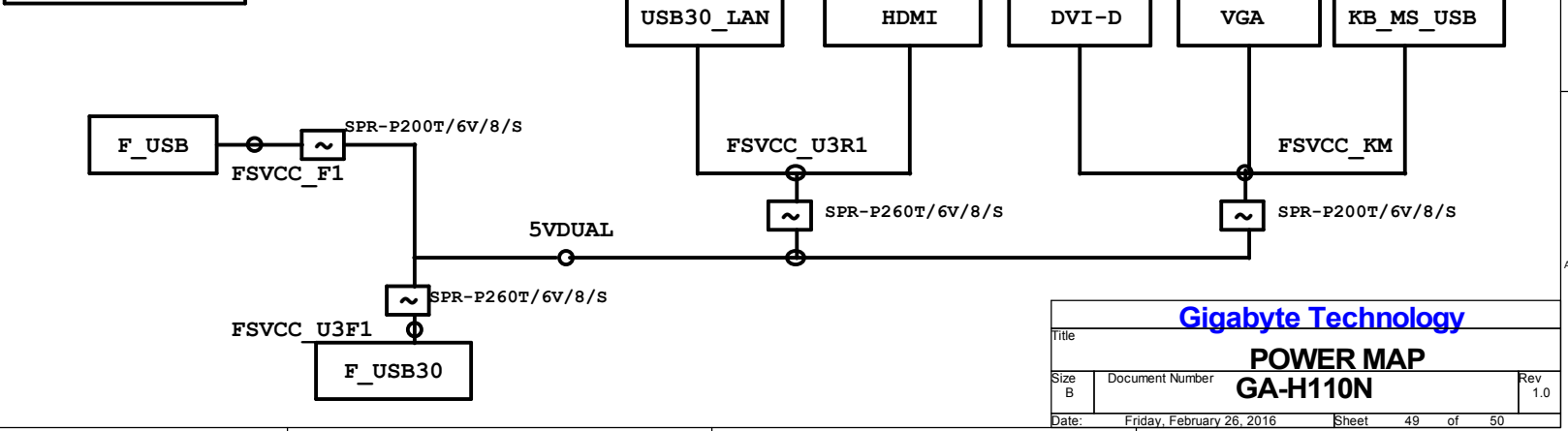
VCORE/VCCGT



POWER



FUSE POWER F/R



PIN NAME	PWR	AFTER	Default	USAGE	NOTE
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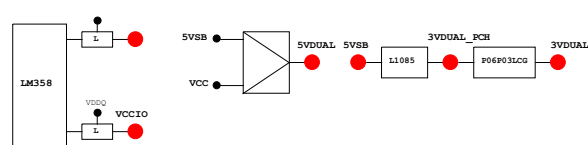
PIN NAME	FW	Default	USAGE	NOTE
GPP_A0	MAIN	NATIVE	N_KERR	P/U 8.2K VCC3
GPP_A1	MAIN	NATIVE	N_LAD0	N/A
GPP_A2	MAIN	NATIVE	N_LXD1	N/A
GPP_A3	MAIN	NATIVE	N_LAD2	N/A
GPP_A4	MAIN	NATIVE	N_LFRM	N/A
GPP_A5	MAIN	NATIVE	N_LFRM	N/A
GPP_A6	MAIN	NATIVE	N_SERIRQ	P/U 8.2K VCC3
GPP_A7	MAIN	NATIVE	N_LDRQ0	P/U 8.2K 3VDDA
GPP_A8	MAIN	NATIVE	N_GPP_A8	P/U 8.2K VCC3
GPP_A9	MAIN	NATIVE	N_LPC2M4	N/A
GPP_A10	MAIN	NATIVE	N_LPC2M4A	N/A
GPP_A11	MAIN	NATIVE	N_P_FHE	P/U 8.2K 3VDDAL_PC
GPP_A12	MAIN	GPI	N_GPP_A12	N/A
GPP_A13	MAIN	NATIVE	N_3_WARN	N/A
GPP_A14	MAIN	NATIVE	N_GPP_A14	P/U 8.2K 3VDDA
GPP_A15	MAIN	NATIVE	N_3_ACK	N/A
GPP_B0	MAIN	CDRE_VID0	N_DCR_VSEL	P/U 8.2K VCC3
GPP_B1	MAIN	CDRE_VID1	N/A	N/A
GPP_B2	MAIN	GPI	N_VRALEST	P/U 8.2K 3VDDAL
GPP_B5	MAIN	GPI	N_PCIE16_PR	P/U 8.2K VCC3
GPP_B6	MAIN	GPI	N_PCIE11_PRR	P/U 8.2K VCC3
GPP_B7	MAIN	GPI	N_PCIE11_PRR2	P/U 8.2K VCC3
GPP_B9	MAIN	GPI	N_PCIE14_PR	P/U 8.2K VCC3
GPP_B10	MAIN	GPI	N/A	N/A
GPP_B11	MAIN	GPO	N/A	N/A
GPP_B12	MAIN	SLP_G0	N/A	N/A
GPP_B13	MAIN	PLTRES	N_PFMST	N/A
GPP_B14	MAIN	H-Z	GPO	N_BFR
GPP_B18	MAIN	H-Z	GPO	N_GPP_B18
GPP_B20	MAIN	MAIN	GPI	N_GPP_B20
GPP_B22	MAIN	MAIN	GPI	N_GPP_B22
GPP_C0	MAIN	SMBCLK	N/A	N/A
GPP_C1	MAIN	SMBDATA	N/A	N/A
GPP_C2	MAIN	H-Z	GPO	N_LPCMC
GPP_C3	MAIN	SMLOCIC	N_SMLOCIC	P/U 499 3VDDAL
GPP_C4	MAIN	SMLODATA	N_SMLODATA	P/U 499 3VDDAL
GPP_C5	MAIN	H-Z	GPO	N_GPP_C5
GPP_C6	MAIN	MAIN	GPI	N_SMLOCIC
GPP_C7	MAIN	MAIN	GPI	N_SMLOCIDAT
GPP_D4	MAIN	MAIN	GPI	N_GPP_D4
GPP_D7	MAIN	MAIN	GPI	N_GPP_D7
GPP_D9	MAIN	MAIN	GPI	N_GPP_D9
GPP_D17	MAIN	MAIN	GPI	N_GPP_D17
GPP_D18	MAIN	MAIN	GPI	N_GPP_D18
GPP_D19	MAIN	MAIN	GPI	N_GPP_D19
GPP_D20	MAIN	MAIN	GPI	N_GPP_D20
GPP_D23	MAIN	MAIN	GPI	N_GPP_D23
GPP_E0	MAIN	NATIVE	N_GPP_E0	P/U 8.2K VCC3
GPP_E1	MAIN	NATIVE	N_GPP_E1	P/U 8.2K VCC3
GPP_E2	MAIN	NATIVE	N_GPP_E2	P/U 8.2K VCC3
GPP_E3	MAIN	GPI	N_CPU_3	P/U 8.2K VCC3
GPP_E4	MAIN	GPI	N_DEVSLP0	P/U 8.2K VCC3
GPP_E5	MAIN	GPI	N_DEVSLP2	P/U 8.2K VCC3
GPP_E7	MAIN	GPI	N_DT_3	P/U 8.2K VCC3
GPP_E8	MAIN	MAIN	N_SATALED	N/A
GPP_E9	MAIN	H-Z	GPI	N_USBC0_F
GPP_E10	MAIN	H-Z	GPI	N_USBC0_R
GPP_E11	MAIN	H-Z	GPI	N_USBC0_R
GPP_E12	MAIN	H-Z	GPI	N_USBC0_F
GPP_F0	MAIN	NATIVE	N_GPP_F0	P/U 8.2K VCC3
GPP_F1	MAIN	NATIVE	N_GPP_F1	P/U 8.2K VCC3
GPP_F2	MAIN	NATIVE	N_GPP_F2	P/U 8.2K VCC3
GPP_F3	MAIN	GPI	N_GPP_F3	P/U 8.2K VCC3
GPP_F4	MAIN	GPI	N_GPP_F4	P/U 8.2K VCC3
GPP_F5	MAIN	GPI	N_GPP_F5	P/U 8.2K VCC3
GPP_F6	MAIN	MAIN	N_DEVSLM	P/U 8.2K VCC3
GPP_F10	MAIN	MAIN	N_GPP_F10	P/U 8.2K VCC3
GPP_F11	MAIN	MAIN	N_GPP_F11	P/U 8.2K VCC3
GPP_F12	MAIN	MAIN	N_GPP_F12	P/U 8.2K VCC3
GPP_F13	MAIN	MAIN	N_GPP_F13	P/U 8.2K VCC3
GPP_F14	MAIN	MAIN	A_SKT00C	P/U 8.2K VCC3
GPP_F15	MAIN	MAIN	N_USBC0_F	N/A
GPP_F16	MAIN	MAIN	N_USBC0_F	N/A
GPP_F17	MAIN	GPI	N_USBC0_R	N/A
GPP_F18	MAIN	MAIN	N_USBC0_F	P/U 8.2K 3VDDA
GPP_F22	MAIN	MAIN	N_GPP_F22	P/U 8.2K VCC3
GPP_F23	MAIN	MAIN	N_GPP_F23	P/U 8.2K VCC3
GPP_G0	MAIN	MAIN	N_GPP_G0	P/U 1K VCC3
GPP_G1	MAIN	MAIN	N_GPP_G1	P/U 1K VCC3
GPP_G12	MAIN	MAIN	N_GPP_G12	P/U 3.3K VCC3
GPP_G16	MAIN	MAIN	N_GPP_G16	N/A
GPP_G18	MAIN	MAIN	N_GPP_G18	P/U 8.2K VCC3
GPP_G19	MAIN	MAIN	N_GPP_G19	P/U 8.2K VCC3
GPP_G20	MAIN	MAIN	N_GPP_G20	P/U 8.2K VCC3
GPP_G21	MAIN	MAIN	N_GPP_G21	P/U 8.2K VCC3
GPP_G22	MAIN	MAIN	N_GPP_G22	P/U 8.2K VCC3
GPP_H0	MAIN	MAIN	M2_CLRSDQ	P/U 8.2K VCC3
GPP_H12	MAIN	MAIN	N_GPP_H12	P/U 8.2K VCC3
GPP_H19	MAIN	MAIN	N_GPP_H19	P/U 8.2K 3VDDA
GPP_H20	MAIN	MAIN	N_GPP_H20	P/U 8.2K 3VDDA
GPP_H21	MAIN	MAIN	N_GPP_H21	P/U 8.2K 3VDDA
GPP_H22	MAIN	MAIN	N_GPP_H22	P/U 8.2K 3VDDA
GPP_I0	MAIN	MAIN	N_HDMI_HDF_F	N/A
GPP_I1	MAIN	MAIN	N_DVI_HDF_F	P/U 1M VCC3
GPP_I2	MAIN	MAIN	N_VGA_HDF_F	N/A

PIN NAME	PWR	AFTER Default	USAGE
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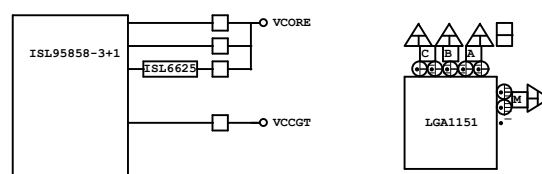
PIN NAME	PWR	TYPE	Default	USAGE
GFP_13	MAIN	GPI	N_GFP_13	P/U 8.2K VCC3
GFP_14	MAIN	GPI	N_GFP_14	P/U 100K GD
GFP_15	MAIN	GPI	N_DDPB_CTRLCLK	P/U 2.2K VCC3
GFP_16	MAIN	GPI	N_DDPB_CTRLDATA	P/U 2.2K VCC3
GFP_17	MAIN	GPI	N_DDPB_CTRLCLK	P/U 2.2K VCC3
GFP_18	MAIN	GPI	N_DDPB_CTRLDATA	P/U 2.2K VCC3
GFP_19	MAIN	GPI	N_DDPD_CTRLCLK	P/U 2.2K VCC3
GFP_110	MAIN	GPI	N_DDPD_CTRLDATA	P/U 2.2K VCC3
GFD0	STBY	BATLOW	N_BATLOW	P/U 8.2K 3VDDAL_PCB
GFD1	STBY	ACPRESENT	N_GD_1	P/U 8.2K 3VDDAL_PCB
GFD2	STBY	LAN_WAKE	N_LAN_WAKE	N/A
GFD3	STBY	FWRBRTN	O_FWRBRTN	P/U 8.2K 3VDDAL_PCB
GFD4	STBY	SLP_S3	N_SLP_S3	N/A
GFD5	STBY	SLP_S4	N_SLP_S4	N/A
GFD6	STBY	SLP_A	N_SLP_A	P/U 8.2K 3VDDAL_PCB
GFD7	STBY	NATIVE	N_S_ACK	N/A
GFD8	STBY	SUSCLK	N_SUSCLK	N/A
GFD10	STBY	SLP_S5	N_SLP_S5	N/A

Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
PCIRST3#/GP10/VDIMM_STR_EN	N/A	
PCIRST2#/GP11	O - PCIE_RST	
PCIRST1#/GP12	O - PFMIRST2	
SVC/PBC1_RQ#/GP14	TPM_GP14	
SLP_SUS#/PCIRST1N#/CIRKX2/GP15	-PCIRSTIN	
PS1_L/FAN_CTL5/CIRKQ2/GP16	N - THERMTKIP	
R12#/GP17	MB_ID2	
THR_PWM_CTL2#/GP20	N - THERMTKIP	
IO_SMI#DCD2#/GP21	❗ PIN	
SP1_S1/GP22	BEEP-	
DPWROR/CPU_DG/GP23	N_PCH_DPWROR	
FAN_TAC5/RTS2#/GP24	❗ PIN	
FAN_TAC4/DSR2#/GP25	FANIO4	
INV_OUT1_SOUT2/GP26	G_PLED	
INV_IN1/SIM2/GP27	INV_IN1	
ATXPG/GP30	PWRK	
CTS1/GP31	CTS1-	
OCMDT3/R11#/GP32	R11-	
OCMDT2/DCD1#/GP33	DCD1-	
VTT_PWRGD/GP34	VTT_PWRGD	
VCC1B_EN/GP35	VCCIO_BN	
FAN_CTL3/GP36	FANPWM3	
FAN_TAC3/GP37	FANIO3	
3VBSW#/GP40	❗ PIN	
OCMDT1/SIN1/GP41	RXD1	
GP42/SCR/FAN_CTL4	❗ PIN	
PANSW#/GP43	-PWRBTSW	
PWRON#/GP44	O_PWRBTSW	
OCMDT0/DSR1#/GP45	DSR1-	
CEZ_N/GP47/JP6	CEB_N	
GP50/JP1	❗ PIN	
FAN_CTL2/GP51	FANPWM2	
FAN_TAC2/GP52	FANIO2	
SUSC#/GP53	N - S4_S5	
PME#/GP54	N - LPCPME	
RSMRST#/CIRKX1/GP55	O - RSMRST	
MCLR/FAN_TAC6/GP56	MCLR	
MDAT/FAN_CTL6/GP57	MDAT	
KCLR/GP60	KCLR	
KDAT/GP61	KDAT	
KBST#/GP62	N - KBSTP	
HOLD_B#/GP63	-SPI_HOLD_B	
HOLD_B#/GP64	-SPI_HOLD_M	
VLDTP_EN/PCH_D0/GP65	❗ PIN	
VCC1_05_EN/GP66	VCC1_0_EN	
GP67	❗ PIN	
USB_F51/P00/GP70	P00	
USB_F52/P01/GP71	P01	
USB_F53/P02/GP72	P02	
USB_F53/P03/GP73	P03	
USB_F55/P04/GP74	P04	
USB_F56/P05/GP75	P05	
USB_F57/P07/GP76	P06	
USB_F58/P08/GP77	P07	
LS_IN1/SLCT/GP80	SLCT	
LS_OUT1/PE/GP81	PE	
LS_IN2/BUSY/GP82	BUSY	
LS_OUT2/ACK#/GP83	ACK-	
IPHONE_CHARGE#/SLINE/GP84	SLIN-	
OC_IN/INIT#/GP85	INIT-	
OC_OUT/AFD#/GP86	AFD-	
USB_OC2/STB#/GP87	STB-	
DDR_EN/GP90	MA_EN	
FWLED/GP91	MGD-	
HOLD_OUT/GP92	❗ PIN	
HOLD_IN/GP93	❗ PIN	
PROCBOOT#/GP94	-PROCBOOT_C0N	
CPUPWRGD/GP95	❗ PIN N_PCH_PWROR	
PCH_VRMPWRGD/GP96	N_PCH_PWRWRGD	
VB_D01/GP97	VB_BD1	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
VCCGT	CPU Graphic Voltage
VCCSA	CPU System Agent Voltage
VCCIO	CPU IO Voltage
VCC1_0_PCH	PCH core
VDDQ	DRAM voltage
VPP_25V	DRAM VPP voltage
DDRVT1	DRAM Termination
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

12SP2-S03507-11R

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	+12V	FANPWM1	FANIO1	IT8628
SYS FAN	FANPWM2	VCC	FANIO2	IT8628
	FAN1_VOUT	N/A	N/A	NCT3941